LOW-VOLTAGE LOW-POWER ANALOG CIRCUIT TECHNIQUES USING FLOATING-GATE MOS TRANSISTORS

By

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TABLE OF CONTENTS

Abstract of Dissertation Presented to the Graduate School
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This research focuses on advanced analog circuit design for low-voltage and low-power applications based on several new techniques using conventional and floating-gate MOS transistors with standard CMOS process technologies.

As a conventional approach which uses standard MOS transistors, a low-voltage current-mode bandgap reference operated with sub-1 V supply is proposed. Also, a new class of low-power analog filters based on charge-transfer amplifiers is introduced. The proposed charge-transfer analog filter can achieve extremely low-power operation.

Another possible approach to achieve low-voltage and low-power operation is to use floating-gate MOS transistors. Analog floating-gate approaches provide many useful options for low-voltage, low-power, and high-precision circuit design. A floating-gate quantized adaptation (FGQA) technique was proposed to implement

high-precision analog circuits by removing analog mismatch errors including process variations. As a practical example of the FGQA technique, an array of 7 adapted current sources was implemented. Experiments show that the output currents of the proposed current sources matched to within 0.1 %, and the adapted currents show significantly improved accuracy compared to the mismatch error of 5 % without adaptation. The accuracy can be improved further by extending the adaptation time.

Recently, a new technique using quasi-floating gate (QFG) MOS transistors has been introduced to simplify initializing floating-gate charge. QFG techniques which can control the initial charge of floating-gate MOS transistors by using quasi-infinite resistors (QIRs) were analyzed to characterize error terms and limitations. Also, several useful quasi-floating gate application circuits, such as QFG multiple-input translinear element circuits, QFG multiple-input CMOS log-domain filters, QFG low-voltage fully-differential amplifiers with QFG common-mode feedback, and a QFG digital-to-analog converter, were demonstrated. Experiments of selected QFG circuits showed very long dc settling behavior with large dc offset. The settling time is reduced when the QFG circuit uses ac inputs or closed-loop structures. Because QFG circuits are based on capacitor coupling, the dc offset occurred by QIRs can be a minor problem.

CHAPTER 1
INTRODUCTION

The importance of low-power analog design continues to increase, for applications such as personal portable devices, biomedical implantable devices, signal processing devices with large arrays, and multimedia systems. Low-power operation of analog integrated circuits can be obtained by decreasing supply voltage and/or bias currents [San99]. Low-voltage design may be more important in analog design than low-power design, because it participates not only for obtaining low-power operation but also for improving circuit performance, which is prone to be degraded by device scaling in advanced sub-micron technologies.

Semiconductor fabrication process technologies have significantly advanced to reduce device sizes and fabrication costs and to increase operating speed. However, device scaling using advanced process technologies brings with many serious problems such as gain reduction, increased mismatch, and reliability problems due to thin gate-oxide thickness [Ste97]. Also, device scaling requires threshold voltage scaling for the continuous use of conventional analog circuits without changing design, because most process technologies limit the maximum applicable supply voltages, (e.g. 2.5 V for 0.25 μm technologies and 1.8 V for 0.18 μm technologies, etc.) Therefore, if scaling down device sizes, supply voltages and threshold voltages is achieved simultaneously, low-voltage circuits are possible with low-power dissipation while maintaining fast operating speed [Yu99].

However, the threshold voltage of CMOS transistors cannot be scaled down without limit. The threshold voltage scaling requires to increase the implant concentration of n(p)-type dopants on p(N)-substrate for N(P)MOSFETs [Kuo99]. However, the high dopant level leads to high substrate capacitance, high substrate leakage current, and relatively low-junction breakdown voltages, and limits threshold voltage scaling down [Nag92].

In addition, many applications require both analog and digital circuits in one chip. Digital circuits have benefit from both low-voltage operation and low-power dissipation, due to zero static currents. Most analog circuits require non-zero static currents because of class A operations with a constant bias. Also, signal swing, dynamic range and signal-to-noise ratio of analog circuits may be significantly degraded by reduced supply voltages and relatively increased noise signals in low-voltage applications [Ram99]. Therefore, performance of analog circuits rarely improves with supply voltage less than 1.8V.

This research focuses on techniques for designing low-voltage and low-power analog circuit blocks based on several new techniques using standard, floating-gate, and quasi-floating gate MOS transistors in standard CMOS technologies.

Chapter 2 presents some conventional low-voltage and low-power techniques which use standard CMOS transistors. Details of low-voltage and low-power limitations of analog circuits including analog mismatch limitations are discussed in Section 2.1 and Section 2.2 [San99, Yan00]. Low-voltage current-mode bandgap reference circuits which can be operated with sub-1 V supply are proposed and

analyzed in Section 2.3. Also, in Section 2.4, the basic operating principle of charge-transfer amplifiers and integrators is introduced [Mar01, Hel76, Kot98], and a new class of low-power analog filters using charge-transfer integrators is suggested [Seo03].

Another possible approach to achieve low-voltage and low-power operation is to use floating-gate MOS transistors, which include a floating capacitor on the gate. Analog floating-gate MOS transistors provide many useful options for low-voltage, low-power, and high-precision analog circuit design, due to their charge storage function and capacitive-computational characteristic [Dio02]. A key practical problem in the floating-gate MOS technique is how to control or program the initial charge of floating-gate nodes [Ber01a, Har01]. In Chapter 3, we review some fundamental advantages of floating-gate MOS transistors, including threshold-voltage control and multiple-input characteristics. Also, some practical techniques to control initial floating-gate charge are discussed.

In CMOS analog circuits, offsets caused by fabrication processing variations can be compensated by adding or subtracting charge on the floating gate of a floating-gate MOS transistor, and high-precision analog circuits can be achieved [Fig00, Fig01, Hyd02]. Chapter 4 introduces a new floating-gate quantized adaptation which can be applied to analog mismatch reduction, to avoid charge-coupling errors occurring as the adaptation circuitry is turned off. The technique is demonstrated with a current source array.

Quasi-floating gates (QFGs) have been suggested as a way to implement many of the functions of floating-gate MOS transistors. A QFG transistor is

implemented by adding elements with extremely high resistance or quasi-infinite resistors (QIRs) between a QFG node and a bias voltage source, instead of the electric isolation of a real floating gate. Several different ways have been suggested to implement these QIRs [Del94, Har02, Nae03, Seo04]. In Chapter 5, basic QIR structures are analyzed and compared, and three sources of error: dc offset, signal distortion, and signal-dependent offset, are defined. Hence, through simulations and experiments, several QIR implementations for various applications are compared. The QFG technique retains many features of floating-gate techniques such as operating-point adaptation and continuous-time capacitive computational, although the technique does not provide long-term charge storage or analog memory. Some examples of low-voltage QFG application circuits are demonstrated.

Many quasi-floating gate circuits can be designed by adapting well-known floating-gate circuits. In Chapter 6, we propose design methods for QFG circuits and some practical QFG application circuits, such as a QFG multiple-input translinear element (MITE) circuit, a QFG multiple-input CMOS log-domain filter, a QFG low-voltage fully-differential operational amplifier with QFG common-mode feedback, and a QFG digital-to-analog converter.

A summary of contributions of this research and suggestions for the future work are summarized in Chapter 7.

CHAPTER 2
LOW-VOLTAGE LOW-POWER ANALOG CIRCUIT DESIGN

2.1 Low-Voltage Low-Power Limitations

2.1.1 Low-Voltage Limitations in Analog Circuit Design

Generally, in analog circuits, all transistors are turned on at the same time. This allows so-called class A, in which signal currents are superposed on constant bias currents. Since most MOS transistors operate in saturation mode, for the input and output circuits as shown in Figure 2-1(A) and (B), the gate-source voltage of an NMOS transistor V_{GS} (or V_{SG} for PMOS) must biased with a voltage larger than the threshold voltage (V_{TH}), and the drain-source voltage (V_{DS}) must be larger than the effective voltage (V_{EFF}) which is the difference of the gate-source voltage and the threshold voltage ($V_{DS} > V_{EFF} = V_{GS} - V_{TH}$). In strong inversion, an effective voltage which is at least 100 ~ 200 mV is used as the quiescent voltage. This basic relationship limits the minimum supply voltage of analog circuits.

The minimum supply range of an analog circuit shown in Figure 2-1(B) is approximately the sum of the threshold voltage magnitudes of an NMOS and a PMOS transistors. However, in digital circuit, the supply voltage limitation is greatly reduced. In a digital circuit, as shown in Figure 2-1(C), even in the case that the supply voltage is less than the minimum requirement, the circuit can still operate because only one transistor is required to operate in saturation mode. Therefore, although CMOS digital circuits can become fairly slow, the circuits will still be

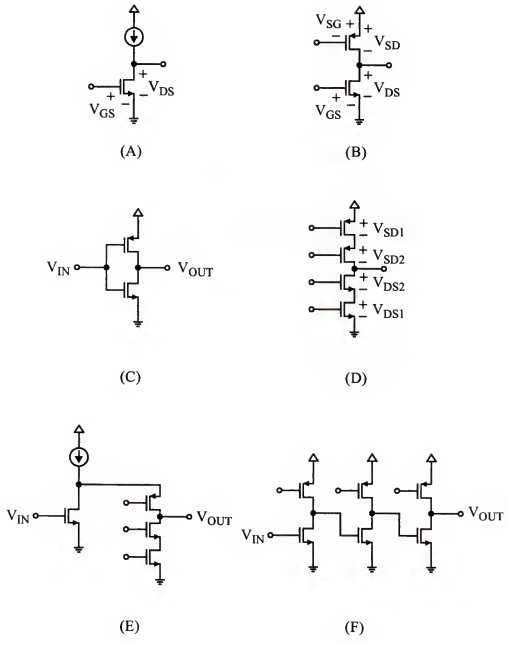


Figure 2-1. Relationship between operating voltage range and supply voltage in CMOS transistors. (A) An input circuit with an NMOS transistor. (B) An output circuit with NMOS and PMOS transistors. (C) An inverter circuit as an example of digital circuits. (D) A cascode output circuit. (E) A folded cascode circuit. (F) A cascade circuit.

functional, while CMOS analog circuits may become nonfunctional in a reduced supply.

In addition, performance improvement in analog circuits usually requires stacked structures. As shown in Figure 2-1(D), the cascode output circuit which uses vertical-stack structures to increase the output resistance and voltage gain is strictly limited to use in the low supply voltage. In low-voltage analog circuits, lateral-stack structures such as folding and cascading may be useful, but they should be used careful because folding and cascading structures may cause additional poles and zeros [Ram99]. Also, the folding and cascoding techniques use extra current paths, as shown in Figure 2-1(E) and (F), which may increase power consumption.

On the other hand, dynamic range in low-voltage circuits is greatly reduced because there is little headroom for signal voltages, and the signal-to-noise ratio is also reduced due to the reduced dynamic range and relatively increased noise. The small bias currents required for small gate-source voltages restrict gain-bandwidth and operating speed [Hui99].

In design using advanced deep sub-micron transistors, supply voltage reduction induces more serious problems, although sub-micron technologies can provide higher frequency operation and less power consumption due to scaled capacitances. Because of the low breakdown voltage caused by thin gate-oxide thickness, it is hard to implement a circuit using voltage-boosting techniques such as voltage doublers and charge pumps [Dic76, Wu98].

A transistor with small feature size is also affected by relatively large mismatch effects, which degrades accuracy [Dre02]. Detailed analysis of mismatch models and their effects will be discussed in Section 2.2.

Therefore, when the supply voltage is reduced to less than sum of the magnitude of the threshold voltages, the small supply voltage makes it very difficult to implement many low-voltage analog building blocks such as low-voltage CMOS analog switches, rail-to-rail amplifiers, constant transconductance amplifiers, and switched-capacitor circuits [Yan00]. Low-voltage analog switches used in discrete-time circuits cannot maintain rail-to-rail operating range [Abo99, Cas91] without special techniques such as internal voltage multiplier [Cas91, Wu98], bootstrapped switch [Abo99, Ste99b], switched op amp [Bas97, Cro94, Dai98, Kar99, Pel98], and modified switched-capacitor integrator [Bid99]. Bandgap reference circuits based on the silicon bandgap voltage of about 1.25 V cannot be implemented with such a sub-1 V supply voltage [Ban99]. So far, numerous techniques to relieve low-voltage limitations have been developed [San99, Yan00, Yu99, Was99]. Among those techniques, we will analyze low-voltage current-mode bandgap reference circuits in Section 2.3.

2.1.2 Low-Power Limitations in Analog Circuit Design

Low-power operation of analog integrated circuits can be obtained by decreasing supply voltage and/or bias currents [San99]. Low-power operation by reducing the supply voltage of analog circuits is discussed in Section 2.1.1. In this section, low-power techniques based on current reduction [Hos80, Vit93a] will be discussed.

All low-power techniques require trade-offs that degrade circuit performance. The most important limitation of low-power analog circuits comes from the need to maintain the energy of the signal much larger than the thermal energy to achieve the required signal to noise ratio (SNR). This condition can be expressed as a minimum power per functional pole, $P_{MIN} = 8kTf(SNR)$, where f is the signal frequency bandwidth, k is Boltzmann's constant (1.38×10^{-23} JK^{-1}), and T is the absolute temperature in Kelvins [Vit94].

In addition, there are several other practical issues in low-power analog design. In saturation, since the transconductance of a MOS transistor decreases approximately in proportion to the square root of its bias current, the speed or frequency response of a circuit with a given capacitance is decreased. The use of a low bias current limits transient characteristics of low-power circuits, including slew rate for large signals and gain-bandwidth for small signals. Also, due to the relatively small signal-to-noise ratio associated with small bias currents, dynamic range and accuracy are also degraded. Therefore, there are unavoidable trade-offs between power and speed, dynamic range, or accuracy [Enz96, Fer01].

In this section, we will briefly review two important low-power techniques, subthreshold-mode operation and charge-transfer amplifier. Among many low-power techniques, subthreshold-mode operation is the most widely-used technique, while the charge-transfer amplifier is a new approach to obtain very low-power circuits.

Subthreshold-mode operation is based on the transistor operation with the gate-source voltage close or lower than the threshold voltage. In this region, a MOS

transistor can be accurately modeled by exponential relationship between its control voltage (gate-source voltage) and drain current, and the drain current is approximately given by Equation (2.1) [Joh97].

$$I_D = I_{D0}\left[\frac{W}{L}\right]\exp\left[\frac{qV_{GS}}{nkT}\right]. \quad (2.1)$$

Where I_{D0} is a process-dependent parameter which depends on V_{SB} and the threshold voltage, W and L are the width and length of a MOS transistor, kT/q is the thermal voltage, and n is a subthreshold slope factor. The behavior of a MOS transistor operated in subthreshold-mode is similar to that of a bipolar transistor, except it has the advantage of a truly negligible dc control current [Vit77]. However, the reduced control of potential causes less-accurate modeling, and reduces transconductance.

Operating MOS transistors in subthreshold mode provides greater power reduction than other techniques because drain currents are small. In subthreshold mode, the transconductance to drain current ratio for a MOS transistor is maximized compared to other operating regions [Vit93b]. However, better gain-bandwidth and noise performance can only be obtained by applying a relatively large drain current [Enz96]. To maintain MOS devices in subthreshold-mode and to keep enough transconductance, very large MOS devices are required. For extremely low-power applications, a small drain current causes low transconductance, which degrades gain-bandwidth and settling time. Therefore, MOS transistors are usually operated in subthreshold mode only for low-frequency, low-power applications.

A lower limit on the gate-source voltage of a MOS transistor operating in subthreshold is determined by the value at which subthreshold currents become comparable to PN junction leakage currents, typically about half of the threshold voltage [Ram99].

Charge-transfer amplifiers are a relatively new class of circuits based on transferring charge between a capacitor placed on the source node and an output capacitor placed on the drain node of a MOS transistor. The charge-transfer amplifier was originally introduced for sense amplifiers in DRAM applications [Hel76], and recently has been applied to comparators in A/D converters [Mar01, Kot98].

A charge-transfer amplifier can achieve extremely low-power operation easily, since it has characteristics of subthreshold-mode operation with minimum transistor sizes, almost zero static power consumption, and is insensitive to bias conditions. However, as we shall see, dynamic performance of charge-transfer amplifiers is limited by offset voltage, residual charge, nonlinearity, charge leakage, and limited speed and frequency response. Most of these problems are not solved yet, and charge-transfer amplifiers are only suitable for low-precision applications. Despite the above problems, the charge-transfer amplifier could provide a solution in some low-power analog and mixed-signal applications.

The operating principle of charge-transfer amplifiers and new switched-capacitor (SC) filter architectures based on charge-transfer amplifiers and integrators will be introduced in Section 2.4 [Seo03].

2.2 Mismatch Limitations

2.2.1 Mismatch Errors in Analog Circuits

The parameters of two identically designed devices on an integrated circuit show a random difference after fabrication, which is called device mismatch. In many analog applications, device matching is a key parameter for precision analog design, because mismatch error helps determine accuracy-speed-power trade-offs [Dre02]. To improve system accuracy, large devices have to be used so that the capacitive loading increases and more power is required to attain a certain speed performance. As a result, matching has a direct impact on the minimum power consumption of high precision circuits [Kin96].

As silicon fabrication technologies move forward, the number of components per chip increases rapidly, and the minimum feature size of transistors continues to decrease. Scaling down of component sizes is necessary, since small-geometry transistors provide small area and the significant improvement of operating speed because of the reduced capacitance. However, decreasing minimum feature sizes corresponds to increasing mismatch, since parameter variations in small-geometry transistors are enlarged [Tul02].

Mismatch in the threshold voltage of MOS transistors is caused by variation of the number of fixed charges in active and depletion regions, and by gate-oxide thickness variation. The charges are implanted, diffused, or generated during fabrication process. The average value is controlled by doping levels. The actual number of carriers in a particular depletion region may differ from the average. The balance of all charges and applied potentials will determine the actual channel

charge in the transistor [Pel99]. Furthermore, mismatch errors become more serious when low-voltage and/or low-power design is required.

2.2.2 Mismatch Analysis Models

Mismatch errors in a circuit are random, and thus cannot be calculated and precisely predicted, and we can only estimate mismatch errors statistically. The estimated value of mismatch errors depends on the assumptions of the applied mismatch model.

Models for mismatch analysis can be divided into two groups [Cro02]. One group is based on complex drain current models like BSIM3 [Dre99, Mic92], and the other is based on simple drain current models [Pel89, Shy84, Vit85]. The former approaches have been shown to give better results for deep sub-micron technologies. However, the models are too complex and inconvenient to use because they contain too many parameters. The latter approaches are simpler and easier to use with relatively less precision. In this section, we will discuss only mismatch models based on a simple drain current, which is enough to show the importance of mismatch errors.

The Pelgrom model [Pel89] is one of the simplest and most widely-used mismatch models. The Pelgrom model is based on three assumptions: (1) the total mismatch of a parameter P is composed of many single events of mismatch generating processes; (2) the effects on the parameter are so small that the contributions to the parameter can be summed; and (3) the events have a correlation distance much smaller than transistor dimensions. From these three assumptions, the Pelgrom model predicts the matching properties of the threshold voltage,

substrate factor, and current factor of MOS transistors as a function of area, distance, and orientation.

The drain current of a long-channel MOS transistor operated in linear region is given by

$$I_D = \beta\left\{\frac{[V_{GS} - V_T - V_{DS}/2]V_{DS}}{1 + \theta[V_{GS} - V_T]}\right\}, \tag{2.2}$$

$$V_T = V_{T0} + K[\sqrt{|V_{SB}| + 2\phi_F} - \sqrt{2\phi_F}], \tag{2.3}$$

$$\beta = \mu C_{OX}(W/L). \tag{2.4}$$

Where β is the current factor, V_T is the threshold voltage, θ represents the effect of mobility reduction and series resistances, K is the body-effect constant, ϕ_F is the built-in potential, and (W/L) is the size of a MOS transistor. In the model, V_{T0}, β, and K are used in the matching description.

The mismatch caused by a parameter P can be expressed in the form of a standard deviation with the spacing factor (D) such as

$$\sigma^2(P) = \frac{A_P^2}{WL} + S_P^2 D^2, \tag{2.5}$$

where A_P is a area proportionality constant for the parameter P, while S_P describes the variation of the parameter P with distance D between devices. Therefore, the mismatch properties of the drain current can be calculated from Equation (2.2) and Equation (2.5),

$$\sigma^2(V_{T0}) = \frac{A_{VTO}^2}{WL} + S_{VTO}^2 D^2, \tag{2.6}$$

$$\sigma^2(K) = \frac{A_K^2}{WL} + S_K^2 D^2, \tag{2.7}$$

$$\sigma^2(\beta) = \frac{A_\beta^2}{WL} + S_\beta^2 D^2, \tag{2.8}$$

where A_{VTO}, S_{VTO}, A_K, S_K, A_β, and S_β are process-related constants.

From Equation (2.6) to Equation (2.8), if W and L are large enough, the relative mismatch in the current factor (β) is approximated to proportional to the inverse-area and distance. The Pelgrom model is valid only for long channel devices.

Another popular mismatch model is the Drennan model [Dre99]. The Drennan model is a mismatch model for MOS transistors based on physical process parameters rather than Spice model parameters in the Pelgrom model. Physical process parameters used in the Drennan model are V_{FB}, T_{OX}, ΔL, ΔW, μ_0, N_{SUB}, ρ_{SH}, and V_{TL}, instead of V_{T0}, β, and K in the Pelgrom model. An advantage of the Drennan model is that it can analyze the contributions of each process parameters to the overall mismatch and identify the most important physical parameter dominating mismatch errors.

2.2.3 Mismatch Reduction Techniques

A general design approach to minimize mismatch errors is to design circuits so that precision is based on the ratio of matched devices rather than on the absolute values of any device parameters. Although all process parameters have random variations, devices which are placed together have the same slow spatial variations, and matching performance between the devices can be significantly improved.

Switched-capacitor circuits and multiple-input floating-gate circuits, which we shall see in Chapter 3, are good examples of the use of matched devices.

The easiest way to reduce mismatch errors is to use larger devices. According to the simple Pelgrom model shown in Section 2.2.2, a two-times improvement of mismatch error in process parameters requires roughly a four-times larger area. However, larger devices include many disadvantages such as larger capacitance, more power dissipation, and high cost.

In layout procedures, to achieve better matching properties, we have to place matching components close together to eliminate spacing-dependent effects, add dummy devices at the outside of device arrays to keep matched devices in the same environmental conditions, use identical wiring for connecting matched devices, use multiples of unity-size devices rather than big devices, and use common-centroid structures. The experiments on Bastos [Bas96] show significant matching improvement due to the very weak influence of process gradients on transistor matching when common-centroid structures are used. In the Bastos model, common-centroid structures were found to have better matching performance than finger-style structures.

The best way to completely minimize mismatch errors is to tune a circuit after fabrication. Recently, some techniques using floating-gate MOS transistors have been reported to compensate analog mismatch errors after fabrication [Dio00, Fig01b, Har01, Has01b, Hye02]. In Chapter 4, a new floating-gate quantization adaptation is proposed to remove main error terms included in the previous techniques.

2.2.4 Mismatch Error Estimation

The practical effects of analog mismatch errors can be estimated under several simple cases. As an example of mismatch estimation, let's consider current mismatch errors of a current mirror pair, which can be an example of an array structure of two identical transistors. Table 2-1 is the current mismatch estimated by applying the Pelgrom model to the experimental data shown in Table 2-2 of a typical 0.25 μm technology. As shown in Table 2-1, to achieve ten times better accuracy, the MOS transistor size of a current mirror pair has to increase by one hundred times.

Also, the mismatch error in the currents increases significantly when the gate-source voltage is reduced, as shown in Table 2-1 and Table 2-2. If the

Table 2-1. Current mismatches of current mirrors estimated by using the Pelgrom model.

L	NMOS			PMOS		
	W_N	V_{GS}=0.5	V_{GS}=1	W_P	V_{SG}=0.5	V_{SG}=1
1 μm	0.42 μm	18.98 %	4.92 %	0.36 μm	17.8 %	4.54 %
	1 μm	11.43 %	3.07 %	1 μm	9.97 %	2.84 %
	2 μm	8.16 %	2.09 %	2 μm	6.77 %	1.91 %
	5 μm	4.84 %	1.23 %	5 μm	4.47 %	1.36 %
1 μm	120 μm	1 %	-	100 μm	1 %	-
	12000 μm	0.1 %	-	10000 μm	0.1 %	-
	8 μm	-	1 %	9 μm	-	1 %
	800 μm	-	0.1 %	900 μm	-	0.1 %

Table 2-2. Current mismatch errors of a current mirror pair measured by using a typical 0.25 μm technology.

L	NMOS			PMOS		
	W_N	V_{GS}=0.5	V_{GS}=1	W_P	V_{SG}=0.5	V_{SG}=1
2 μm	0.42 μm	13.42 %	3.48 %	0.36 μm	12.59 %	3.21 %
	1 μm	8.08 %	2.17 %	1 μm	7.05 %	2.01 %
	2 μm	5.77 %	1.48 %	2 μm	4.79 %	1.35 %
	5 μm	3.42 %	0.87 %	5 μm	3.16 %	0.96 %

threshold voltage mismatch and the current factor mismatch of a simple current mirror are uncorrelated, the standard deviation of drain current mismatch is given by

$$\sigma(ID) = \sqrt{\sigma^2(\beta) + \left[\frac{g_m}{I_D}\sigma(V_T)\right]^2}. \tag{2.9}$$

From Equation (2.9), the drain current mismatch in weak inversion (large g_m/I_D) becomes

$$\sigma(ID) = \frac{g_m}{I_D}\sigma(V_T), \tag{2.10}$$

while the drain current mismatch in strong inversion (small g_m/I_D) is given by

$$\sigma(ID) = \sigma(\beta). \tag{2.11}$$

Therefore, for low-voltage and low-power analog design, the mismatch error term can be a dominant design factor, and it will be hard to reduce. [Enz96]

2.3 Low-Voltage Current-Mode Bandgap Reference

2.3.1 Current-Mode Bandgap Reference Circuit

Bandgap references provide a regulated voltage, which is stabilized over supply voltage and temperature variations. In bandgap reference circuits, a regulated output voltage is obtained from the weighted sum of the thermal voltage of kT/q and the built-in voltage of a diode [Joh97], because the thermal voltage has a positive temperature coefficient, while the built-in voltage has a negative temperature coefficient. The regulated output voltage of a bandgap circuit based on silicon process is about 1.25 V, and required minimum supply voltage usually must be larger than this. This is a major limitation of voltage-mode bandgap references.

To implement a bandgap reference circuit with a supply voltage less than the silicon bandgap voltage, a current-mode bandgap reference circuit can be used. In a current-mode bandgap reference, the output voltage is generated by the sum of two currents, one proportional to the thermal voltage and another proportional to the built-in voltage of a diode. A current-mode bandgap circuit was originally proposed by [Ban99], and recently, another circuit with minor modification of the original idea was introduced [Ytt03]. The circuit proposed in [Ban99] was simulated for the supply voltages above 0.84 V, but was measured only above 2.1 V. The bandgap circuit had given a stable output reference voltage of 515 $\pm$ 1 mV in the supply range from 2.2 to 4.0 V at 27 ^{o}C, and 515 $\pm$ 3 mV in the temperature range from 27 to 125 ^{o}C. The equivalent temperature sensitivity is calculated to 117 ppm/^{o}C. The bandgap reference circuit proposed in [Ytt03] had reported simulated temperature sensitivity of 93 ppm/^{o}C over the temperature range from -40 to 100 ^{o}C.

However, the current-mode bandgap circuit in [Ban99] has three main disadvantages for practical applications. In the following section, we will analyze these problems, and suggest solutions for the successful implementation of a sub-1 V current-mode CMOS bandgap reference circuit.

2.3.2 Conventional Current-Mode Bandgap Reference Circuit

The current-mode bandgap reference originally proposed by [Ban99] is shown in Figure 2-2. The detailed schematic is shown in Figure 2-3. When the resistors R_1 and R_2 are equal, and the op amp is in correct operating region, the

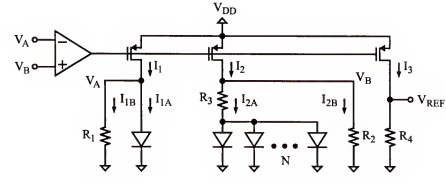


Figure 2-2. The current-mode bandgap reference circuit proposed by [Ban99].

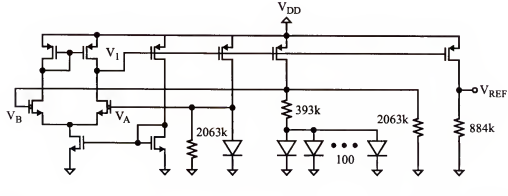


Figure 2-3. The schematic of a conventional current-mode bandgap reference circuit.

currents, I_1, I_2, and I_3 become equal to each other, and the regulated output voltage can be represented as

$$V_{REF} = R_4 I_3 = R_4[I_{2A} + I_{2B}] = R_4\left[\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3}\right]. \qquad (2.12)$$

The built-in potential of the diode, V_{f1}, has a negative temperature coefficient, and dV_f has a positive temperature coefficient, since it is proportional to the thermal voltage V_T.

The current-mode bandgap reference circuit shown in Figure 2-3 was proposed in two different versions, one for simulation, and another for measurement version. The simulation version uses low-threshold-voltage transistors, which have threshold voltages of -0.3 V for PMOS and 0.4 V for NMOS. The measurement version circuit used normal threshold voltage transistors with threshold voltages of -1.0 V for PMOS and 0.7 V for NMOS. Also, depletion-type NMOS devices with threshold voltage of -0.2 V were used for differential input transistors of the op amp.

The minimum supply voltages of these circuits are limited by the minimum supply voltage of the op amp or the relationship between the input common-mode voltage range of the op amp and the diode voltage. Considering the temperature variation of -10 to 125 ^{o}C, the worst case (largest diode voltage) should be at the lowest temperature, because the diode voltage has a negative temperature coefficient, and the maximum diode voltage becomes about 0.9 V at -10 ^{o}C. Therefore, at the worst case, the minimum supply voltages are approximately given by

$$V_{DD,MIN,S} = V_f - V_{THN} - V_{THP} = 0.9 - 0.4 + 0.3 = 0.8, \quad (2.13)$$

for the simulation version, and

$$V_{DD,MIN,M} = V_f - V_{THI} - V_{THP} = 0.9 - (-0.2) + 1.0 = 2.1, \quad (2.14)$$

for the measurement version. Therefore, Banda's circuit shown in Figure 2-3 was simulated in the supply voltage range above V_{DD} = 0.84 V, and measured in the supply range from 2.2 to 4.0 V and temperature variation from 27 to 125 °C.

The first problem of the circuit shown in Figure 2-3 is the use of depletion-type transistors for op amp input devices. The depletion-type NMOS devices which have a negative threshold voltage can increase the minimum supply voltage. From Equation (2.14), if normal or low threshold voltage NMOS devices were used for input devices, the minimum supply voltage is reduced from 2.1 V to 1.2 V or 1.5 V. Depletion-type MOS devices are not available in most CMOS processes. Nevertheless, the depletion-type devices are unavoidable in the circuit shown in Figure 2-3, because of the input common-mode voltage range of the op amp.

The circuit in Figure 2-3 consists of two feedback loops which participate to force the same voltage on op amp input nodes, denoted by V_A and V_B, and to maintain equal currents, I_1, I_2, and I_3. Due to temperature variations, the diode voltage varies between 0.4 ~ 0.9 V. To keep the feedback loop gain large enough, the input common-mode range of the op amp must cover the whole diode voltage range for given temperature variations. The minimum diode voltage must be larger than the threshold voltage of an input NMOS transistor. Therefore, the circuit

shown in Figure 2-3 has to include depletion-type NMOS input transistors, and hence, the minimum supply voltage is increased to 2.1 V.

The second problem is that the circuit can have multiple operating points [Fox98]. The simulation version of the circuit which uses NMOS input devices with 0.4 V threshold voltages can be operated with a sub-1 V supply voltage. However, due to wide-varying diode voltages and the narrow input common-mode range of the op amp, the circuit can bias into an unusable operating point. Whenever the diode voltage deviates from the input common-mode range of the op amp, the op amp output gain decreases abruptly, and the diode turns off with diode voltage close to zero. Therefore, in the op amp and the diode, only leakage currents can flow, and an undesired operating point exists. Because the simulation version circuit has the minimum supply voltage of less than 1 V and a narrow input common-mode voltage range, the undesired stable operating point can easily appear.

To avoid the undesired operating point, the input common-mode range of the op amp should cover all of the diode voltage range from 0.4 to 0.9 V. The measurement version of the circuit in Figure 2-3 can have a wide input common-mode voltage range because of the depletion-type input devices. However, because of the depletion-type input devices, sub-1 V operation is impossible. In the simulation version, because of the undesired operating point, the circuit cannot operate reliably.

The another problem of the circuit is the use of impractically large resistors. The circuit in Figure 2-3 uses two resistors of over 2 MΩ, which are much to big to implement with predictable values in practical circuits.

2.3.3 Proposed Current-Mode Bandgap Reference Circuit

The main issues required to design this sub-1-V current-mode bandgap reference are how to keep the op amp in correct operation and to maintain feedback loops having their loop gain high enough.

As a first step of design, careful analysis of the minimum supply voltage of the op amp is required, since the minimum supply voltage of the current-mode bandgap circuit is limited by both the supply voltage and the diode voltage. The minimum supply voltage of a simple low-voltage op amp shown in Figure 2-4 is the larger voltage of

$$V_{DD} > V_{DS,SAT5} + V_{DS,SAT1} + V_{DS,SAT3} + |V_{TP3}|,$$

$$= 3V_{DS,SAT} + |V_{TP}|, \tag{2.15}$$

and

$$V_{DD} > V_f - (V_{DS,SAT2} + V_{TN2}) + V_{DS,SAT2} + V_{DS,SAT3} + |V_{TP3}|$$

$$= V_f - V_{TN2} + V_{DS,SAT3} + |V_{TP3}|$$

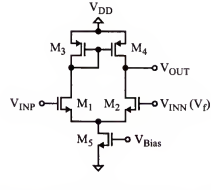


Figure 2-4. A simple operational amplifier.

$$= V_f - V_{TN} + V_{DS,SAT} + |V_{TP}|. \quad (2.16)$$

If $V_{DS,SAT}$ is assumed as 100 mV, $V_{f,MAX}$ = 0.9 V in the worst case, and we use the low threshold voltage transistors of V_{TN} = 0.3 V and V_{TP} = -0.3 V, the minimum V_{DD} becomes 1.0 V from Equation (2.16). Also, for normal threshold voltage devices which have V_{TN} = 0.7 V and V_{TP} = -0.7 V, the minimum V_{DD} is still 1.0 V. However, in this case, because $V_{f,MIN}$ is about 0.4 V and the input voltage of the op amp should be larger than the minimum input common-mode range, the 0.3 V shift of V_f is required. Therefore, if we add a voltage shifter between V_f and V_{IN}, we can design a sub-1 V bandgap reference without depletion-type input devices, even without any low threshold voltage transistors. Also, the voltage shifter can be easily implemented using resistors.

Next, to eliminate any unstable and/or undesired operating points, the stabilizing circuit shown in Figure 2-5 is proposed. The stabilizing circuit consists of three transistors and is connected to the inverting input of the op amp. When the bandgap reference circuit is under correct operation, V_A is in the range from 0.4 ~ 0.9 V, and the stabilizing circuit is inactive. When V_{DD} is 1.0 V, the voltage

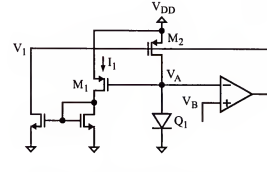


Figure 2-5. The stabilizing circuit.

difference between V_{DD} and V_A is 0.1 ~ 0.6 V. Therefore, if the threshold voltage of M_1 is greater than the voltage between V_{DD} and V_A, the stabilizing circuit will be off, and does not affect the main circuit. However, if an undesired operating point exists, the diode Q_1 would be off, and V_A would drop close to 0 V, so that the voltage between V_{DD} and V_A would become close to V_{DD}, larger than the threshold voltage of M_1. In that case, M_1 would turn on, and I_1 would be generated. Then, V_1 could provide the gate voltage of M_2, and hence, the diode would turn on and V_A would be in the correct range with desired operating point. The positive feedback loop would be active, and the main circuit can be operated correctly. Therefore, no undesired operating points exist. After obtaining the desired operating point of the feedback loops, the stabilizing circuit will automatically returns off.

High-valued resistors can be avoided by scaling the bias currents and the ratio of R_2 and R_3 in Equation (2.12). Equation (2.12) can be expressed as

$$V_{ref} = R_4\left[\frac{V_{f1}}{R_2} + \frac{dV_f}{R_3}\right] = \frac{R_4}{R_2}\left[V_{f1} + \frac{R_2}{R_3}dV_f\right] = \frac{R_4}{R_2}\left[V_{f1} + \frac{R_2}{R_3}V_T \ln\frac{A_2}{A_1}\right]. \quad (2.17)$$

If the diode current ratio of A_2/A_1 is decided, and the maximum resistance value ($R_1 = R_2$) is selected to a reasonable value, R_3 can be obtained by using the temperature dependence of thermal voltage and built-in diode voltage with the relationship of

$$R_3 = R_2\left[-\frac{\Delta V_T/\Delta T}{\Delta V_{f1}/\Delta T}\ln\frac{A_2}{A_1}\right] = R_2 \ln 100\left[-\frac{\Delta V_T/\Delta T}{\Delta V_{f1}/\Delta T}\right]. \quad (2.18)$$

After that, we can choose R_4 from the desired output reference voltage.

Therefore, if we choose the current ratio of A_2/A_1 equal to 100 and R_1 (= R_2) is 50 kΩ, from the temperature dependence of $\Delta V_{f1}/\Delta T$ = -1.566 mV/°C and $\Delta V_T/$

ΔT = 0.086 mV/°C from a given model parameters. From Equation (2.18), R_3 is determined by 13 kΩ. Also, R_4 is fixed to 22 kΩ for the desired output reference voltage of 550 mV and I_3 of 25 μA. By using TI 0.5 μm process with low threshold voltage transistors, a new current-mode bandgap reference circuit was designed, as shown in Figure 2-6.

In addition, the proposed bandgap reference circuit in Figure 2-6 can be modified to a version that uses normal threshold voltage transistors by adding voltage shifters as shown in Figure 2-7. If a fabrication process does not allow the low threshold voltage transistors, the additional voltage shifters with voltage drop of 0.3 V can be inserted above both diodes to hold the diode voltage in the input common-mode range. Of course, in this case, the minimum supply voltage will be increased by the voltage drop of the voltage shifters. In the Figure 2-7, the resistors of R_5 and R_6 are given by

$$R_5 = R_6 = \frac{V_{TN} + 2V_{DS,SAT} - V_{f,MIN}}{I}. \tag{2.19}$$

Therefore, we can design the bandgap reference circuits with the minimum supply

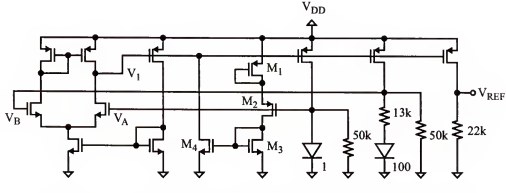


Figure 2-6. The proposed current-mode bandgap reference circuit.

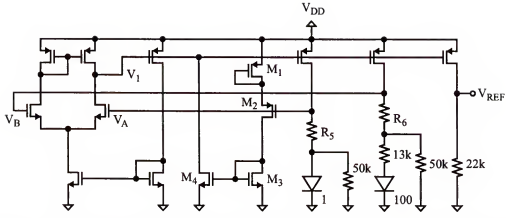


Figure 2-7. The bandgap reference circuit of the normal threshold voltage devices.

Table 2-3. The simulation results of the multiple operating points.

	Stable / Unstable	V_A / V_B
Conventional Circuit Without the Stabilizing Circuit in Figure 2-3.	Stable (desired)	740 mV
	Stable (undesired)	143 μV
	Unstable	396 mV
Proposed Circuit With the Stabilizing Circuit in Figure 2-6.	Stable	740 mV

voltage of less than 1 V using low threshold voltage devices and with the minimum supply voltage of about 1.2 V using normal threshold voltage devices.

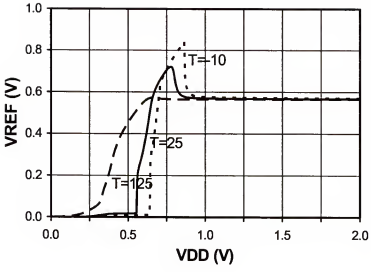
To verify the multiple operating points of the current-mode bandgap reference circuit, the operating points of the simulation version shown in Figure 2-3 and the proposed circuit in Figure 2-6 which includes the stabilizing circuit are simulated. The results shown in Table 2-3 indicate that the circuit with the stabilizing circuit has only one stable operating point, and that the circuit without the stabilizing circuit has three operating points, including two stable (desired and undesired) and one unstable operating points.

Showing the positive feedback loop gain of less than unity can also prove the existence of multiple operating points. The loop gain of the circuit shown in Figure 2-3 has two gain stage, one comes from the op amp and the other comes from the PMOS devices placed above the diodes. At the desired operating point, the loop gains of the positive and negative feedback are calculated by SPICE simulation as 54.65 (V/V) and -256 (V/V).

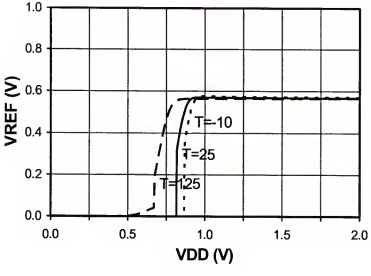
On the other hand, at the undesired stable operating point, since the two input nodes of the op amp have the same resistance values and the PMOS transistors placed in the path of the diodes are identical, we can simulate the loop gain by finding the transfer function from one input node to another input node of the op amp or vice versa. In this case, the positive and negative feedback loop gains have the same magnitude as 0.16 (V/V), and these can satisfy the assumption of less than unity.

Therefore, the minimum supply voltage of the circuit in Figure 2-6 which uses low threshold voltage devices can be less than 1 V, and the circuit using normal threshold voltage devices, shown in Figure 2-7, can have the minimum supply voltage about 1.2 V. The output reference voltages of the current-mode bandgap reference circuit can have any value from 0 to V_{DD} as determined by the ratio R_4/R_2.

Figure 2-8 shows simulation results of the regulated output reference voltages of Figure 2-6 and Figure 2-7 with $R_5 = R_6 = 1\ k\Omega$. For the low threshold voltage version, the output voltage is 568 ± 2.3 mV in the range of $V_{DD} = 1 \sim 2$ V and $T = -10 \sim 125\ ^{o}C$, while the normal threshold voltage version gives the output of



(A)



(B)

Figure 2-8. The output reference voltages of the proposed low-voltage current-mode bandgap reference circuits. (A) Using low threshold voltage transistors. (B) Using normal threshold voltage transistors.

Table 2-4. The comparisons of the current-mode bandgap references.

	Banba Simulation	Banba Measure.	Ytterdal [Ytt03]	Proposed Low V_{TH}	Proposed Normal V_{TH}
V_{TN}	0.4 V	0.7 (- 0.2) V	0.42 V	0.304 V	0.745 V
V_{TP}	- 0.3 V	- 1.0 V	- 0.39 V	- 0.385 V	0.731 V
$V_{DD,MIN}$	0.84 V	2.1 V	0.6 V	0.8 V	1.0 V
V_{DD} range	-	2.2 ~ 4 V	0.6 ~ 1.2 V	1 ~ 2 V	1 ~ 2 V
Temp. range	-	27 ~ 125 °C	-40 ~ 100 °C	-10 ~ 125 °C	-10 ~ 125 °C
V_{REF}	-	515±3 mV	400±2.6 mV	568±2.3 mV	567±2.1 mV
Sensitivity	-	117 ppm/°C	93 ppm/°C	81 ppm/°C	74 ppm/°C

567 ± 2.1 mV in the same range. Table 2-4 shows the comparison of the results with the other current-mode bandgap reference circuits. In Table 2-4, the bandgap circuit proposed by [Ytt03] shows a minimum supply voltage of 0.6 V. The circuit in [Ytt03] was implemented using low threshold voltage transistors, and has the same structure as the proposed bandgap reference shown in Figure 2-6, except it used bulk-driven MOS transistors for op amp input devices. Although bulk-driven MOS transistors can relax the input common-mode limitation in the op amp, such devices have large noise and leakage current. Also, bulk-driven operation is possible only in twin-well processes.

As shown in Table 2-4, both low and normal threshold voltage versions of proposed current-mode bandgap reference circuits shows similar or better performance comparing with others, and they can reduce the threshold voltage limitations of low-voltage bandgap reference circuits.

2.4 Low-Power Charge-Transfer Analog Filters

2.4.1 Charge Transfer Amplifier

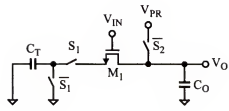
A CTA is an amplifier operated by the charge transfer mechanism between a transferring capacitor (C_T) placed on the source and an output capacitor (C_O) placed on the drain node of a MOS device.

The CTA was originally introduced for sense amplifiers in DRAM applications [Hel76], and recently has been applied to comparators in A/D converters [Mar01, Kot98]. The CTA could be a good solution to achieve extremely low-power operation easily since it has characteristics of the subthreshold-mode operation with minimum transistor size, almost zero static power consumption, and insensitivity to bias conditions.

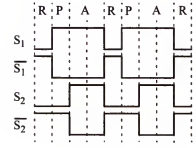
In this section, new CTA architectures which can be used to implement switched-capacitor integrators and filters are introduced and explored, and the design method of a new SC filter family based on the CTA is proposed.

2.4.2 Operation of Charge Transfer Amplifier

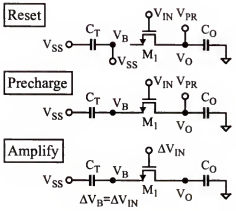
As shown in Figure 2-9, charge transfer occurs in three clock phases: reset, precharge, and amplify phases. In the reset phase (S_1 off and S_2 off), C_T is discharged to zero and C_O is precharged to a precharge voltage (V_{PR}) typically around half of the supply voltage. Next, in the precharge phase (S_1 on and S_2 off), C_T charges to the source voltage (V_B) which equals the input reference voltage (V_{IN}) minus the threshold voltage (V_{TH}) of NMOSFET M_1, operated as a source follower. In the amplify phase (S_1 on and S_2 on), for any positive change in the input voltage (ΔV_{IN}), NMOS M_1 turns on and charge $C_T \Delta V_{IN}$ flows from C_O to C_T



(A)



(B)



(C)

Figure 2-9. Basic operations a charge transfer amplifier. (A) Schematic of an NMOS CTA. (B) Clock timing used in the CTA. (C) CTA operations.

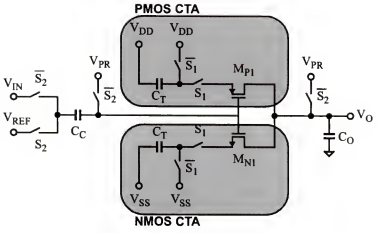
in common-gate mode. Neglecting variation of M_1's V_{TH}, the output voltage variation (ΔV_O) equals $-C_T\Delta V_{IN}/C_O$, independent of the bias conditions and device parameters. Thus, the CTA can obtain fairly accurate values of gain with an open-loop structure.

The CTA provides very low power consumption because of its small switching and precharging power dissipation and nearly zero static power consumption. The actual average power consumption of a CTA is proportional to the clock frequency because the static period is shorter in the high clock frequency. In addition, the CTA provides several advantages compared with conventional SC amplifiers, such as the simplicity of design and immunity from fluctuations in bias conditions and device parameters.

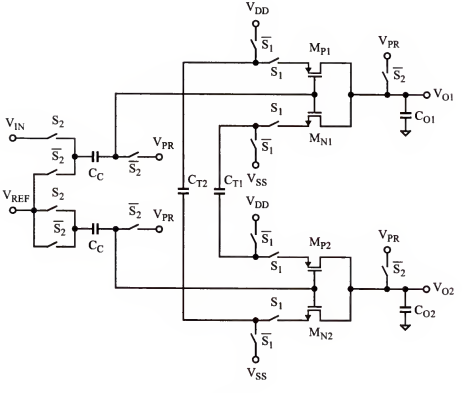
As described so far, CTAs also have some serious limitations such as input polarity problems (positive input changes only for NMOS and negative changes for PMOS CTAs), offset voltages caused by residual precharge current and drain leakage, and gain nonlinearity due to body effect. To remove the input polarity problem, a CMOS CTA that includes both NMOS and PMOS CTAs as shown in Figure 2-10(A) can be used. The differential CMOS CTA (DCTA) shown in Figure 2-10(B) can further reduce offsets and nonlinearity [Mar01].

2.4.3 Switched-Capacitor Filters using Charge Transfer Integrator

The output capacitor (C_O) in the CMOS CTA shown in Figure 2-10 is precharged to the V_{REF} during every reset and precharge phase. If a switch is added as shown in Figure 2-11, to isolate C_O in the reset phase, C_O will retain charge from



(A)



(B)

Figure 2-10. (A) A CMOS charge transfer amplifier. (B) A CMOS differential charge transfer amplifier.

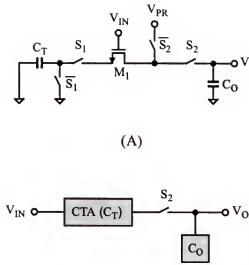


Figure 2-11. (A) A charge transfer integrator (CTI). (B) A CTI symbol.

each previous cycle, and the circuit operates as a charge transfer integrator (CTI). Neglecting bulk effect and other non-ideal effects, the transfer function of CTI is

$$C_O V_O(z) = C_O z^{-1} V_O(z) - C_T V_{IN}(z), \tag{2.20}$$

$$H_{CTI}(z) = \frac{V_O(z)}{V_{IN}(z)} = -\frac{C_T}{C_O}\frac{1}{1-z^{-1}}. \tag{2.21}$$

The CTI is an open-loop structure with no virtual ground node, and so has limited linearity. The dynamic range of a CTI is further limited by the imperfect charge transfer caused by the finite duration of amplify phase.

2.4.4 Switched-Capacitor CTI Filters

Figure 2-12(A) is a general first-order switched-capacitor filter with an inverting input (C_1/C_A) and a feedback (C_2/C_A) integrator. The ideal transfer function is given by

$$H_{1,SC}(z) = \frac{V_O(z)}{V_{IN}(z)} = -\frac{C_1 z}{(C_A + C_2)z - C_A}. \tag{2.22}$$

The transfer functions of CTA filters can be derived in the same way as for conventional switched-capacitor filters. The transfer function of first-order CTA filter shown in Figure 2-12(B) and Figure 2-12(C) is

$$H_{1,CTA}(z) = -\frac{(C_1/C_A)z}{(1 + C_2/C_A)z - 1} = H_{1,SC}(z). \tag{2.23}$$

For the second-order CTA filter shown in Figure 2-13, the transfer function is given by

$$H_{2,CTA}(z) = -\frac{(C_1C_5/C_A^2 - C_2/C_A)z + (C_2/C_A)z^2}{1 + (C_4C_5/C_A^2 - C_6/C_A - 2)z + (1 + C_6/C_A)z^2}. \tag{2.24}$$

Equation (2.24) is a typical second-order SC filter transfer function, except that Equation (2.24) has no highpass signal path [Joh97]. This is only a minor limitation

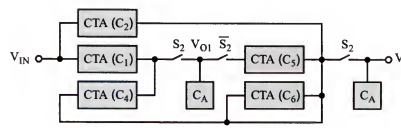


Figure 2-13. A second-order CTA SC filter.

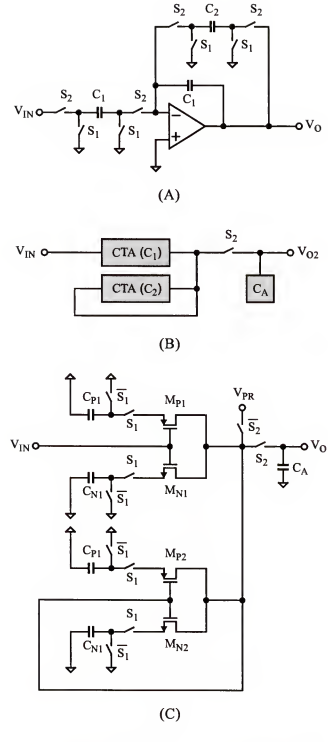


Figure 2-12. A first-order CTA SC filter. (A) SC prototype. (B) Block diagram. (C) Schematic.

since most filter applications are lowpass and bandpass.

The practical filter coefficients in the transfer functions Equation (2.23) and (2.24) are given by ratios to the integrating (output) capacitor and determined by the filter characteristics [Joh97]. For the first-order lowpass filter,

$$C_1 = C_2 = \frac{2\pi(F_P/F_S)}{1-\pi(F_P/F_S)}C_A, \tag{2.25}$$

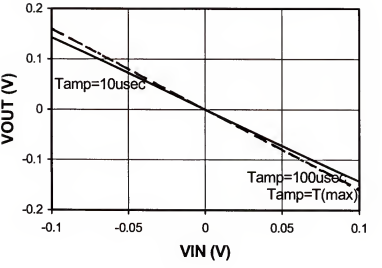
where F_P is the 3dB bandwidth frequency and F_S is the sampling frequency of the CTA SC filter. For the second-order filter,

$$C_4 = C_5 = \frac{2\pi(F_P/F_S)}{\sqrt{1-\pi(F_P/F_S)/Q+\pi^2(F_P/F_S)^2}}C_A, \tag{2.26}$$

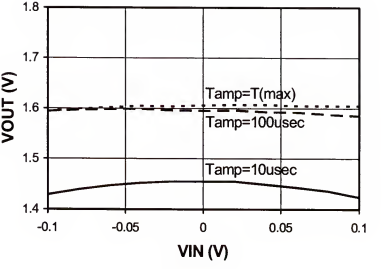
$$C_6 = \frac{C_4^2}{2\pi(F_P/F_S)QC_A}, \tag{2.27}$$

where Q is the quality factor of bandpass filter. For the lowpass, C_2 should be set to zero and input capacitor C_1 is chosen to set passband gain, while for the bandpass filter, C_1 is set to zero and C_2 is used to set gain. Note that the gain reduction in CTA filters comes from offset voltage error and body effects and can be compensated in part by scaling integrator capacitors. Therefore, the design of CTA SC filters is straightforward and similar to conventional SC filter design.

Before analyzing the CTA filters, it is worthwhile to verify the linearity of DCTAs, limited by body effects and incomplete charge transfer. As shown in Figure 2-14, for the fixed reset and precharge phase, the voltage gain according to the amplify phase was simulated. Simulation shows the DCTA can achieve up to 40dB



(A)



(B)

Figure 2-14. DCTA output linearity. (A) Output voltage. (B) DC gain linearity.

dynamic range of 140 mV input voltage range with an amplify phase of 10 μsec and 200 mV input voltage range with the amplify phase of 100 μsec.

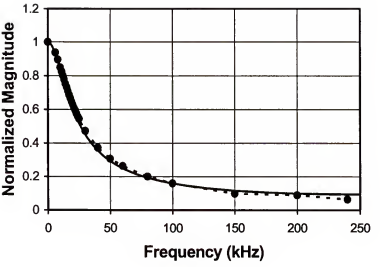
To demonstrate the new CTA SC filter architectures, three SC filters based on differential CTIs were designed and simulated, including first-order lowpass, second-order lowpass, and second-order bandpass filters. The circuits were simulated in HSPICE using BSIM models for IBM 6HP CMOS 0.25μm parameters. The supply voltage was 2.5 V.

The sampling frequency was 500 kHz, the 3dB bandwidth of the lowpass filters was 15kHz (F_P/F_S = 0.03), and the bandpass filter center frequency was 50kHz. The Q of the second-order bandpass filter was 10 and Q for the lowpass filter was 0.707. The capacitor values used in the filter design are shown in Table 2-5. HSPICE was used to simulate frequency responses for the CTA SC filters, and the simulation results are compared with ideal transfer functions obtained from MATLAB simulations.

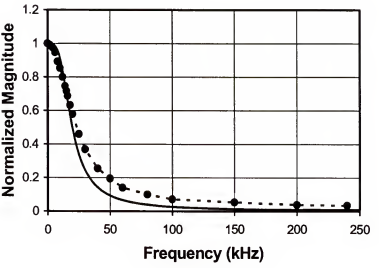
As shown in Figure 2-15, the frequency responses of CTA filters agree well with the ideal cases, except for the Q value of the bandpass filter. The power dissipation of DCTA filters was simulated at the sampling frequencies of 500 kHz and 50 kHz, and as shown in Table 2-6, the total power dissipations were 1.9, 4.0,

Table 2-5. The practical capacitor values used in the CTA SC filters.

Sets	C_A	C_1	C_2	C_4	C_5	C_6
1-LPF	2.000pF	0.183pF	0.183pF	-	-	-
2-LPF	1.600pF	0.202pF	-	0.202pF	0.202pF	0.308pF
2-BPF	1.600pF	-	0.500pF	0.608pF	0.608pF	0.059pF

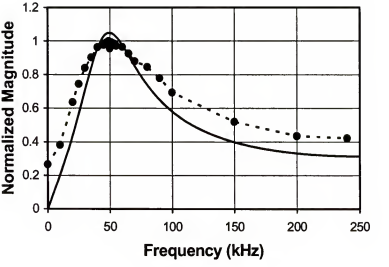


(A)



(B)

Figure 2-15. Frequency responses of CTA SC filters (solid line, MATLAB; dotted line; Hspice results). (A) 1st-order low-pass filter. (B) 2nd-order low-pass filter. (C) 2st-order band-pass filter with Q=1. (D) 2st-order band-pass filter with Q=10



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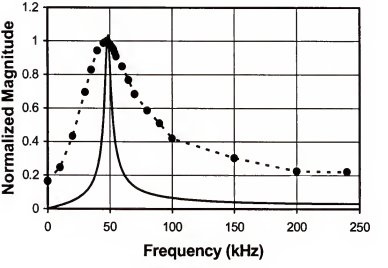


(D)

Figure 2-15. Continued.

Table 2-6. The simulation results of the power computation of CTA SC filters.

F_S	Sets	$P(V_{DD})$	$P(V_{REF})$	$P(V_{SW})$	P(Total)
500kHz	1-LPF	1.738 μW	0.021 μW	0.142 μW	1.901 μW
	2-LPF	3.663 μW	0.056 μW	0.317 μW	4.037 μW
	2-BPF	5.492 μW	0.047 μW	0.556 μW	6.094 μW
50kHz	1-LPF	0.187 μW	0.004 μW	0.012 μW	0.202 μW
	2-LPF	0.407 μW	0.007 μW	0.043 μW	0.457 μW
	2-BPF	0.620 μW	0.006 μW	0.032 μW	0.658 μW

and 6.1 μW for 500 kHz clock frequency and 0.20, 0.46, and 0.66 μW for 50 kHz clock frequency for the first-order and the second-order lowpass and second-order bandpass filters. The simulations show that the CTA SC filters could be adapted to implement low-frequency, modest-performance, and low-cost analog sampled-signal circuits with extremely low power consumption.

Figure 2-16 shows the layout of the three DCTA SC filters which were laid out by using IBM 6HP 0.25 μm process. The active chip areas are just 0.056 mm^2 for first order and about 0.12 mm^2 for second-order filters.

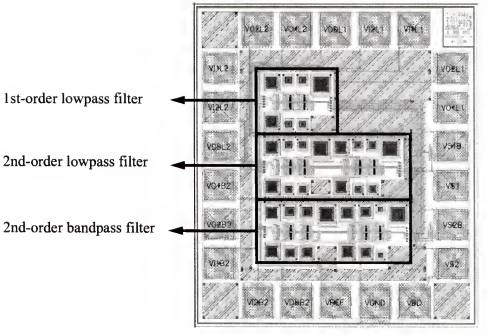


Figure 2-16. Layout of DCTA SC filters.

CHAPTER 3
FLOATING-GATE CMOS TRANSISTOR

3.1 Floating-Gate CMOS Technique

3.1.1 Floating-Gate CMOS Transistor

The first Floating-gate MOS (FGMOS) transistors were reported in the mid 1960s, and the first commercial product, an EPROM (erasable programmable read only memory), was introduced in 1971 using a FAMOS (floating-gate avalanche-injection MOS) transistor [Fro71, Len69]. FGMOS transistors have been used as memory elements in many digital systems. Since the stored charge on a floating gate is an analog quantity, if the floating-gate charge could be controlled with sufficient precision, the FGMOS transistor can apply to many analog applications, including analog memory storage, threshold voltage control, error trimming, and analog adaptation. These analog floating-gate approaches provide useful options for low-voltage, low-power, and high-precision analog applications.

Applications of floating-gate CMOS transistors are divided into three major areas, which are analog memory elements, adaptive circuit elements, and capacitive computational. Floating-gate transistors can be applied to long-term nonvolatile storage devices, because the floating gate is electrically isolated unless a high voltage bias is applied. By adding a programming procedure, the amount of stored charge on the floating gate can be controlled and used to set an effective threshold voltage or to compensate analog errors. Also, floating-gate circuits can be designed

to allow continuous-time adaptation between incoming and outgoing signals at the floating-gate node, which can be used for the continuous adaptation of dc operating points and removing dc offsets of amplifiers. In addition, another useful feature of floating-gate devices is that floating-gate circuits can be used for continuous-time capacitive-computational circuits. Unlike resistor-based circuits or switched-capacitor circuits, continuous-time capacitive-computational circuits use capacitors as precise elements in the continuous time domain.

Floating-gate transistors can extend the usage of capacitors, which provide high impedance at low frequency, high linearity, and excellent accuracy with good matching properties, compared with other passive elements in fabrication processes. Capacitors can be used for voltage-dividers to set precise operating points and to implement analog computations. Combining voltage-division elements with feedback yields a capacitive-computational feedback amplifier whose gain is determined by a precise capacitor ratio. Also, as we shall see in Section 3.1.3, floating-gate transistors can be used in multiple-input structures, which provide useful options in analog computation including addition and subtraction of voltages, and may more functions in the current domain. However, voltage-division structures based on only capacitors create a floating node, and controlling floating-gate node charge is a key problem.

The basic structure of a FGMOS transistor is shown in Figure 3-1. The internal floating-gate node is completely electrically isolated for dc. The floating gate is connected to the control-gate, drain, source, and substrate, with capacitors denoted as C_{FG}, C_{GD}, C_{GB}, and C_{GS}, respectively, as shown in Figure 3-1.

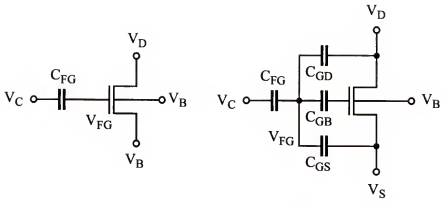


Figure 3-1. The basic structure of a floating-gate MOS transistor and parasitic capacitors.

The effective threshold voltage at the control gate is

$$V_{T,EFF} = \frac{C_T}{C_{FG}} V_T + \frac{Q_{FG}}{C_{FG}} - \frac{C_{GD}}{C_{FG}} V_{DS} - \frac{C_{GB}}{C_{FG}} V_{BS}, \tag{3.1}$$

$$C_T = C_{FG} + C_{GD} + C_{GS} + C_{GB}, \tag{3.2}$$

where Q_{FG} is the initial charge stored on the floating-gate, and C_T is the total capacitance. From Equation (3.1), the effective threshold voltage strongly depends on the drain voltage. However, if $C_{FG} >> C_{GD}$, C_{GS}, C_{GB}, and $C_T \sim C_{FG}$, Equation (3.1) becomes

$$V_{T,EFF} \cong V_T + \frac{Q_{FG}}{C_{FG}}, \tag{3.3}$$

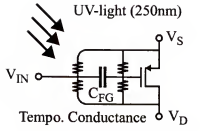
and the effective threshold voltage can be adjusted by controlling the stored charge on the floating-gate, Q_{FG}.

3.1.2 Initial Charge Control

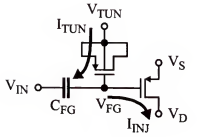
One practical problem of the floating-gate technique is how to control or program the initial charge of floating-gate nodes. For the precise control of the floating-gate charge, we need a way to add and remove charge from the floating gate. Three techniques, UV-conductance processing [Ber01a], Fowler-Nordheim tunneling plus hot-electron injection [Har01], and the quasi-floating gate technique [Del94, Seo04], have been reported.

UV-conductance processing is used to control the initial floating-gate charge without any additional on-chip programming circuitry. As shown in Figure 3-2(A), when the gate-source/gate-drain regions are exposed to UV-light (250 nm), a UV-activated conductance temporarily connects the source and drain to the floating gate [Ben93]. By using metal layers as a shield, we may activate UV-conductance between source/drain terminals and floating gates of desired transistors. The UV-activated conductance disappears when the UV-light is removed. However, UV-conductance processing is expensive, and makes it difficult to reprogram the floating-gate charge. Also, in some processes, the gate is not fully transparent to UV light. Furthermore, all of the floating-gate transistors must be programmed simultaneously, so individual tuning of the floating-gate transistors is not possible.

Fowler-Nordheim tunneling and hot electron injection can be used to implement high precision circuits because of their bi-directional adaptation and re-programming ability. Fowler-Nordheim tunneling [Len69, Sze81] is used to increase floating-gate charge by removing tunneling electrons from the floating-gate to an external voltage source through a tunneling junction, as shown Figure 3-



(A)



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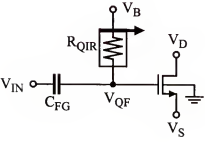


(C)

Figure 3-2. Methods to control the initial charge of floating-gate nodes. (A) UV-conductance processing. (B) Fowler-Nordheim tunneling plus hot-electron injection. (C) Quasi-floating gate technique.

2(B). If a positive high voltage applied to across the tunneling junction, the voltage difference between both the sides of the tunneling junction increases the effective electric field across the gate-oxide. Therefore, the probability of electron tunneling through the oxide barrier is increased, and electron tunneling occurs. Impact-ionized hot-electron injection (IHEI) [Dio97] is used to decrease floating-gate charge. In a FGMOS transistor, channel holes can collide with the drain lattice if they are accelerated in the channel-to-drain junction. When the channel-to-drain voltage becomes large, the channel holes collide with enough energy to liberate electron-hole pairs in the drain, and generate ionized electrons. The ionized electrons are injected from the drain to the floating-gate because of the high channel-to-drain voltage. Also, if gate-to-channel polarity is large, these electron can be injected into the gate. However, Fowler-Nordheim tunneling and hot-electron injection require external high voltages. Another problem of the Fowler-Nordheim tunneling and hot-electron injection is charge redistribution that occurs when turning off tunneling and injection voltage sources.

In the quasi-floating gate technique shown in Figure 3-2(C), the floating gate is no longer purely isolated but weakly electrically connected by using a very large or "quasi-infinite resistor" (QIR). This technique can provide a well-defined dc operating point without requiring additional post-processing or high-voltage programming circuitry. However, precise biasing using quasi-floating gate techniques is limited by offset voltages caused by substrate leakage currents and input signals. Also, the quasi-floating gate technique provides no storage functions

[Seo04]. Detailed discussions of the quasi-floating gate technique and application circuits will be presented in Chapter 5 and Chapter 6, respectively.

A detailed review of Fowler-Nordheim tunneling and hot electron injection techniques and the conventional floating-gate adaptation (FGA) procedure using the balance of tunneling and injection currents will be in Section 3.2. Section 3.3 will show simulation models and model parameters for tunneling and injection currents of floating-gate MOS transistors. A simulation-parameter extraction circuit and parameter-extraction procedures are also introduced in Section 3.3.

3.1.3 Multiple-Input Floating-Gate MOS Transistor

FGMOS transistors are often used as a multiple-input floating-gate MOS (MIFG-MOS) transistor, as shown in Figure 3-3. The MIFG-MOS transistor retains several advantages compared to a single input FGMOS transistor. In a MIFG-MOS transistor, each input node can be used as a control input to adjust the desired effective threshold voltage of a MIFG-MOS transistor for low-voltage applications.

The charge stored on the floating-gate node is derived from the capacitive-coupling relation as Equation (3.4).

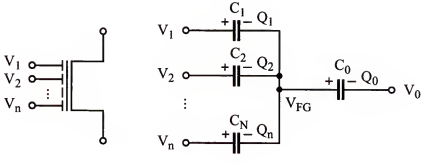


Figure 3-3. The structure of a multiple-input floating-gate MOS transistor.

$$Q_{FG} = Q_0 + \sum_{i=1}^{n}(-Q_i) = C_0(V_{FG} - V_0) + \sum_{i=1}^{n} C_i(V_{FG} - V_i)$$

$$= \sum_{i=0}^{n} C_i(V_{FG} - V_i) = V_{FG}\sum_{i=0}^{n} C_i - \sum_{i=0}^{n} C_i V_i, \qquad (3.4)$$

where Q_0 is the initial charge stored in the floating-gate node, and V_i's and C_i's are the input voltages and input capacitors of a MIFG-MOS transistor. Therefore, from Equation (3.4), the floating-gate voltage of a MIFG-MOS transistor is represented by the initial floating-gate charge and input potentials as Equation (3.5).

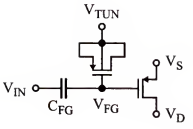
$$V_{FG} = \frac{Q_{FG} + \sum_{i=0}^{n} C_i V_i}{\sum_{i=0}^{n} C_i} = \frac{Q_{FG} + C_0V_0 + C_1V_1 + C_2V_2 + \ldots + C_nV_n}{C_0 + C_1 + C_2 + \ldots + C_n}. \qquad (3.5)$$

Because a multiple number of input signals can be easily connected to a single transistor, the MIFG-MOS transistor provides some useful options to achieve various arithmetic functions in signal processing circuits. Some arithmetic signal-processing circuits and log-domain filters using multiple-input translinear elements (MITEs) will be discussed in Chapter 6 as examples of MIFG-MOS transistors.

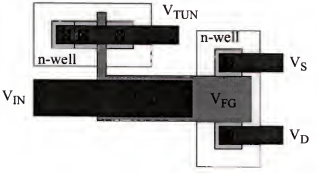
3.2 Floating-Gate Adaptation Using Tunneling and Injection

3.2.1 Fowler-Nordheim Tunneling

Fowler-Nordheim tunneling [Len69, Sze81] is used to increase charge (remove electrons) on the floating-gate of a floating-gate MOS transistor. The charge on the floating-gate is increased by removing tunneling electrons from the



(A)



(B)

Figure 3-4. A schematic and layout of a tunneling junction which is implemented by using a drain-source-well shorted PMOS transistor, and connected to the floating-gate. (A) Schematic. (B) Layout.

floating-gate to an external voltage source through a tunneling junction. The tunneling junction shown in Figure 3-4 is usually implemented using a drain-source-well shorted PMOS transistor, and connected to a floating gate. If a positive high voltage is applied to tunneling junction, the voltage difference between the tunneling bias and the floating-gate increases the effective electric field across the oxide. Therefore, the probability of electron tunneling through the oxide barrier is increased, and hence, electron tunneling occurs.

The tunneling current is given by

$$I_{TUN} = -I_T \exp\left[\frac{E_0}{E_{OX}}\right] = -I_T \exp\left[\frac{t_{OX}E_0}{V_{OX}}\right], \tag{3.6}$$

$$V_{OX} = V_{TUN} - V_{FG}, \tag{3.7}$$

where I_T is a pre-exponential constant, t_{OX} is the gate-oxide thickness, V_{OX} is the oxide voltage, V_{TUN} is the tunneling voltage, E_{OX} is the oxide electric field, and E_0 is a device parameter which is roughly equal to 25.6V/nm [Mea94, Dio02]. The typical value of the oxide field ranges from 0.75 to 1.0V/nm [Has01a]. The gate current caused by the tunneling current is simplified to

$$I_G = I_T \exp\left[\frac{-V_F}{V_{OX}}\right], \tag{3.8}$$

where V_F is a constant that depends on oxide thickness [Dio02].

3.2.2 Impact-Ionized Hot-Electron Injection

Impact-ionized hot-electron injection (IHEI) [Dio97] is used to decrease charges (add electrons) on the floating-gate of a floating-gate MOS transistor. In a floating-gate PMOS transistor, channel holes can collide with the drain lattice if they are accelerated in the channel into the drain depletion region. If the channel-to-drain voltage becomes large enough, the channel holes collide with a sufficient energy, and then, liberate electron-hole pairs in the drain generate ionized electrons. The ionized electrons are injected from the drain to the floating-gate because of the high channel-to-drain voltage. The gate current due to the IHEI is given by

$$I_G = \beta I_S \exp\left[\frac{V_{CD}}{V_{INJ}}\right], \tag{3.9}$$

where I_G is the gate current, I_S is the source current, V_{CD} is the channel-to-drain

voltage, β and V_{INJ} are fitting constants determined by the process. The injection current shown in Equation (3.9) excludes channel-to-gate voltage dependences because IHEI depends only weakly on this channel-to-gate voltage [Dio00].

The tunneling current and the injection current oppose each other. Therefore, from Equations (3.8) and (3.9), the total floating-gate current is given by

$$I_G = \beta I_S \exp\left[\frac{V_{CD}}{V_{INJ}}\right] - I_T \exp\left[\frac{-V_F}{V_{OX}}\right]. \tag{3.10}$$

The total floating-gate current strongly depends on V_{INJ} and V_F, respectively.

3.2.3 Floating-Gate Adaptation Circuit

The goal of floating-gate adaptation (FGA) is to adjust a floating-gate voltage to a particular voltage that provides a desired threshold voltage or a desired drain current of a floating-gate transistor. Since IHEI is more suitable for precise control than tunneling, adaptation using IHEI after tunneling is preferred.

One simple example of the FGA is the self-convergent analog memory cell shown in Figure 3-5 [Fig01a]. In Figure 3-5, when a reference current source is

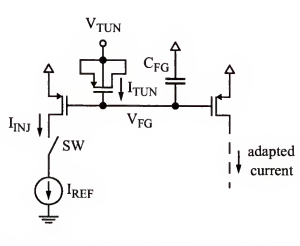


Figure 3-5. A schematic of a simple floating-gate adaptation circuit.

applied to the drain of a floating-gate PMOS transistor, the floating-gate voltage is adapted to the final voltage which is fixed to the source-gate voltage determined by the reference current. After adaptation, the adapted floating-gate voltage has a nonvolatile charge storage, and is shared with the target transistor (right-hand side) so that the target transistor has a drain current equal to the reference current.

The detailed adaptation procedure is as follows: First, turn on the tunneling voltage until the floating-gate voltage becomes larger than the final voltage, so that the source-gate voltage is smaller and the source-drain voltage is larger than the final voltages. The high source-drain voltage allows IHEI from the drain to the floating-gate, and the floating-gate voltage starts to decrease. When the floating-gate voltage reaches the final voltage, which is fixed by the bias current, the increased drain voltage turns off the IHEI process.

However, any procedure of turning off the adaptation circuitry causes charge-coupling errors which will change the adapted voltage on the floating-gate. In the circuit in Figure 3-5, for example, when the switch in the injection path is turned off, the change of the floating-gate voltage is approximately

$$\Delta V_{FG} = \frac{C_{GD}}{C_{GD} + C_{FG}} \Delta V_D, \tag{3.11}$$

where ΔV_D is the change of the drain voltage when turning off the injection switch.

As a simple estimate of the charge coupling error, if we assume that the source-drain voltage required for injection is about 3 V and the gate-drain capacitance is 10 fF, the variation of the floating-gate voltage induced by the charge injection can be estimated as 3 mV when C_{FG} = 1 pF. To eliminate this charge

coupling error that occurs when the adaptation is turned off, a new floating-gate adaptation algorithm called floating-gate quantized adaptation (FGQA) will be proposed in Chapter 4.

3.3 Simulation of Floating-Gate MOS Transistors

3.3.1 Floating-Gate Transistor Simulation Model

Simulation of floating-gate circuits is not easy because of the lack of simulation parameters for tunneling and injection processes. An empirical simulation model of a floating-gate PMOS adaptation circuit was proposed in [Rah02]. In the model, the tunneling and injection currents are modeled as voltage-controlled-current-sources as shown in Figure 3-6. A voltage-controlled-voltage-source is added to allow a circuit simulation to converge with a floating node. The voltage source does not change any properties in the circuit because there will be no current flow in the resistor connected between the floating-gate and the voltage source. However, this method is only available for transient simulation. In dc simulation, the voltage-controlled-voltage-source produces positive feedback with unity gain, and the dc operating point cannot converge to a fixed value.

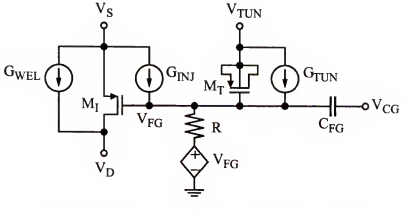


Figure 3-6. A simulation model of a floating-gate PMOS adaptation circuit.

The Fowler-Nordheim tunneling current that increases charges on the floating gate is determined by the voltage between the tunneling junction and a constant V_F which depends on oxide thickness. From Equation (3.8), the tunneling current is given by

$$I_{TUN} = -I_{TUN0} WL \exp\left[\frac{-V_F}{V_{OX}}\right], \tag{3.12}$$

where I_{TUN0} is the pre-exponential current.

For the injection current, because there is no simple model for the IHEI current which decreases the charge on the floating gate, a semi-empirical equation given in Equation (3.13) is used to model the injection current.

$$I_{INJ} = \alpha I_S \exp\left[-\frac{\beta}{(V_{GD}+\delta)^2} + \lambda V_{SD}\right], \tag{3.13}$$

where I_S is the source current, and α, β, and δ are fitting parameters which depend on the process.

Impact ionization in the channel-to-drain depletion region generates additional electron-hole pairs. The electrons tend to be collected by the well and the holes by the drain. This impact ionization current can also be modeled using a semi-empirical equation given by

$$I_{WELL} = \eta I_S V_W \exp\left[\frac{-\lambda'}{V_W}\right], \tag{3.14}$$

$$V_W = \gamma V_{SD} - \kappa V_{SG} + V_{TH}, \tag{3.15}$$

where η, γ, κ, and λ' are fitting parameters.

The model parameters used in Equations (3.12) ~ (3.15) are process-dependent and must be determined by experiments.

3.3.2 Parameter Extraction Circuit Design

A parameter extraction circuit shown in Figure 3-7 was designed to measure the parameters of floating-gate adaptation circuits using IBM6HP 0.25 μm technology. Figure 3-8 shows a detailed schematic of the parameter extraction circuit.

In the circuit shown in Figures 3-7 and 3-8, if there are no tunneling and injection currents (i.e. V_{TUN} = 0 V and V_{SD} = 0 V), the floating-gate voltage is expressed by

$$V_{FG} = \frac{C_A V_{OUT} + C_{GD} V_D + C_{GS} V_S + Q_0}{C_A + C_{GD} + C_{GS}} = \frac{C_A V_{OUT} + Q_0}{C_A}, \qquad (3.16)$$

where Q_0 is the initial charge stored on the floating gate. The floating-gate voltage

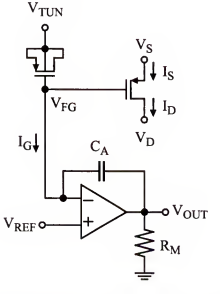


Figure 3-7. A parameter extraction circuit to measure simulation parameters of tunneling and injection currents in floating-gate adaptation circuits.

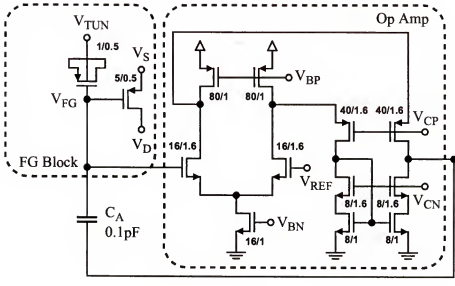
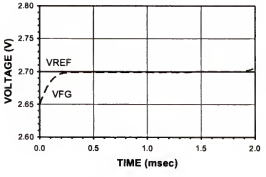


Figure 3-8. A detailed schematic of the simulation-parameter extraction circuit.

is a constant, but unknown value. If V_{TUN} or V_{SD} becomes positive, tunneling or injection current is generated and appears in the gate current. The gate current can be inferred from the change of the voltage across feedback capacitor C_A, as shown in Equation (3.17).

$$I_G = C_A \frac{\Delta V_{OUT}}{\Delta t}. \tag{3.17}$$

Figure 3-9 and Figure 3-10 illustrate the procedure for measuring tunneling and injection currents. As shown in Figure 3-9(A) and Figure 3-10(A), the reference voltage (V_{REF}) must initially be set to a slightly larger value than the floating-gate voltage (V_{FG}) in the tunneling current measurement, while V_{REF} must be set initially to a slightly smaller value than V_{FG} in the injection current measurement. This allows the operational amplifier to operate in its active region while the output varies according to Equation (3.17). Therefore, we must know the initial floating-



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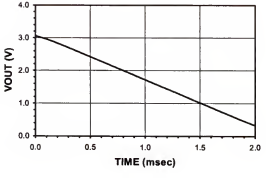

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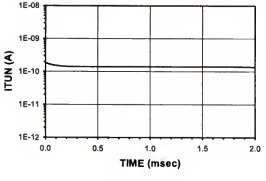
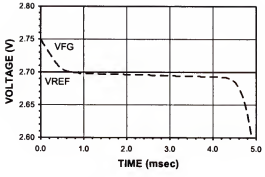
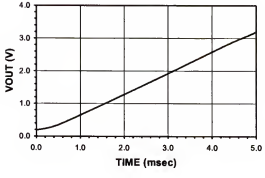


(C)

Figure 3-9. Simulation of the procedure of tunneling-current measurement. (A) Reference voltage and floating-gate voltage. (B) Output voltage of the parameter extraction circuit. (C) Tunneling current.



(A)



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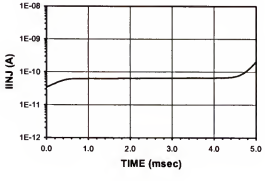


(C)

Figure 3-10. Simulation of the procedure of injection-current measurement. (A) Reference voltage and floating-gate voltage. (B) Output voltage of the parameter extraction circuit. (C) Injection current.

gate voltage, which takes on an unknown value during the fabrication and packaging processes. The floating-gate voltage can be found by sweeping V_{REF}.

In the design, careful consideration for selecting the value of C_A is required to ensure a convenient measurement time period. If we expect the gate currents between 1 pA and 1 aA and choose C_A = 0.1 pF,

$$\left[\frac{\Delta V_{OUT}}{\Delta t}\right]_{MAX} = \frac{I_{G,MAX}}{C_A} = \frac{1pA}{0.1pF} = \frac{1V}{0.1sec}, \tag{3.18}$$

$$\left[\frac{\Delta V_{OUT}}{\Delta t}\right]_{MIN} = \frac{I_{G,MIN}}{C_A} = \frac{1aA}{0.1pF} = \frac{1\mu V}{0.1sec} = \frac{1V}{28hour}. \tag{3.19}$$

As shown in Figure 3-8, an NMOS folded-cascode op amp is used in the circuit, and the performance of the op amp is shown in Table 3-1. To ensure the accuracy of measurements which require a long measuring period, estimation of the

Table 3-1. Performance of the NMOS folded-cascode op amp in the simulation-parameter extraction circuit.

Performance	Simulation
$(W/L)_{INPUT}$	16 μm/1.6 μm
$I_{D,INPUT}$	60 μA
DC Gain	3.82 kV/V (~72 dB)
R_{OUT}	9.40 MΩ
G_m	0.406 mA/V
3-dB Bandwidth	1.85 MHz
Unity Gain Frequency	1.23 GHz
Phase Margin	60 °
Output Equivalent Thermal Noise	1.049 pV^2/Hz (1.024 μV/rt-Hz)
Output Equivalent 1/f Noise @ 1Hz	371.8 nV^2/Hz (609.8 μV/rt-Hz)

total accumulated noise during the measuring period is necessary. As shown in Equation (3.20), the total accumulated noise can be obtained by integrating the output equivalent noise voltages of thermal and flicker noises during total measuring time.

$$\bar{v}_n^2 = \int_{f_L}^{f_H} \left[\bar{v}_{Thermal}^2 + \frac{\bar{v}_{1/f}^2}{f} \right] df, \tag{3.20}$$

where f_H is the 3dB bandwidth (1.85 MHz) and f_L is the inverse of the maximum expected measuring time period (28 hours). From Equation (3.20), the total accumulated noise voltage is estimated to 2 mV for 0.1 sec period and to 2.5 mV for 28 hour period. If we use the output voltage change of 1V, the measurement has 0.2 ~ 0.25 % error terms. Therefore, the total accumulated noise is small enough, and are not significantly changed according to the measurement periods.

3.3.3 Tunneling and Injection Parameter Extraction

Using the parameter extraction circuit shown in Figure 3-7, the tunneling current was measured with respect to the various oxide voltages (V_{OX}), which are the difference of the external tunneling voltage (V_{TUN}) and the floating-gate voltage. The square dots in Figure 3-11 are measured tunneling currents, and the solid line is tunneling currents calculated by using Equation (3.12) and tunneling constants. The tunneling constants were obtained by comparison with the measured data such that I_{TUN0} is 5.6 x 10^7 (A/m^2) and V_F is -368 (V) for the given 0.25 μm process.

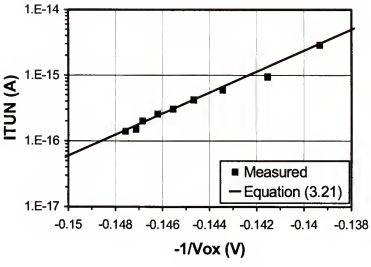
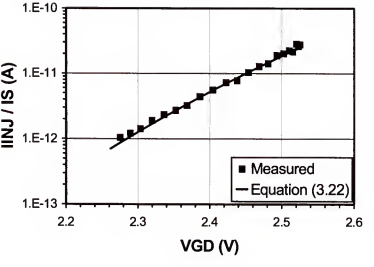
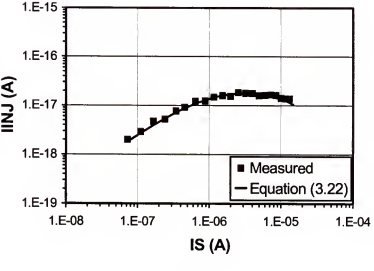


Figure 3-11. The measured tunneling current with respect to the various high external tunneling voltage.

The injection current was measured with a source-drain voltage of 3.3 V. Figure 3-12 shows the measured injection currents with respect to the gate-drain voltage and the source current for a fixed source-drain voltage. The square dots are measured injection currents, while the solid-line is tunneling currents calculated by using Equation (3.13). The fitting parameters obtained from the measured data were $\alpha = 4.55 \times 10^{-5}$, $\beta = 160$ (V^2), $\delta = 0.48$ (V), and $\lambda = 1$.



(A)



(B)

Figure 3-12. The measured injection currents. (A) Injection current vs. gate-drain voltage. (B) Injection current vs. source current.

CHAPTER 4
FLOATING-GATE QUANTIZED ADAPTATION

4.1 Introduction

MOS transistor matching is one of the most important issues in analog integrated circuits. Performance of high-precision analog circuits depends on the matching properties of individual components [Dre02]. In advanced deep sub-micron technologies, device matching becomes more important because of the reduced device feature size and the increased process variations [Tul02].

In analog circuits, offset is defined as the non-zero-mean value of the difference between many pairs of components, while mismatch refers to the stochastic spread of standard deviations [Pel99]. Therefore, offset can represent overall mismatch errors, including area mismatches, threshold voltage mismatches, and process parameter variations. The overall offset of a circuit can be compensated by adding or subtracting charges on the floating gate of a floating-gate MOS transistor using Fowler-Nordheim tunneling and impact-ionized hot electron injection [Har01], and hence, high precision analog circuits are obtained.

One problem in the adaptation processes using tunneling and hot-electron injection is charge re-distribution after the adaptation procedure is turned off. This charge-coupling error may significantly degrade the accuracy of the adapted circuit.

In this chapter, a new floating-gate adaptation (FGA) technique called floating-gate quantized adaptation (FGQA) is introduced. In Section 4.2, floating-

gate quantized adaptation (FGQA) is introduced, including FGQA current sources as an example. Section 4.3 analyzes error terms in the FGQA technique, including quantization errors. In Section 4.4, a high-precision current source array using FGQA techniques, which can be directly applied to an n-bit thermometer-code current steering D/A converter, is designed, simulated, and measured.

4.2 Floating-Gate Quantized Adaptation

4.2.1 Charge Coupling Errors in the Adaptation Process

Charge-coupling errors caused by turning off the adaptation circuitry were introduced briefly in Section 3.2.3. Practical effects of such errors are illustrated using a simulated current-adaptation circuit, as shown in Figure 4-1.

The current adaptation procedure is as follows: (1) a high tunneling voltage (V_{TUN} = 10 V) is applied to generate a tunneling current at the floating gate, which increases the floating-gate voltage (V_{FG}); (2) after a long-enough tunneling period, the floating-gate voltage is high enough to ensure the drain voltage (V_1) is below

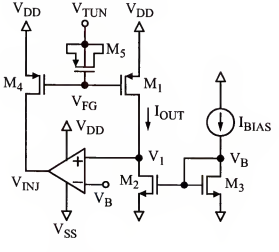


Figure 4-1. A floating-gate adaptation circuit for generating an identical current source.

the target voltage (V_B); (3) after that, V_{TUN} drops to V_{DD} (3.3 V) to turn off the tunneling process; (4) an Injection-On voltage is applied ($V_{INJ} = V_{INJ,ON} = -3.3$ V) to turn on the injection process; (5) in the injection process, the negative differential input of a comparator forces the comparator output to the negative supply rail (V_{SS}), and the high source-drain voltage of the injection MOS transistor, M_4 ($V_{DD} - V_{SS}$); (5) if the input offset voltage of the comparator is negligible, the negative feedback loop forces the drain voltage of M_1 (V_1) to equal the target voltage (V_B), and the output current (I_{OUT}) is adapted to the same value as the bias current (I_{BIAS}); (6) if $V_1 > V_B$, (the adaptation process is complete,) V_{INJ} is set to 0 V (or V_{DD} or any voltage higher enough to turn off injection), and injection process is turned off.

Charge-coupling errors occur when the tunneling or injection voltages change. Although the tunneling voltage change is large, the charge-coupling problem of tunneling-off can be eliminated if the tunneling period is long enough so that the floating-gate voltage is high oven after the charge coupling. However, the charge-coupling error caused by turning off injection is more serious because it occurs after each step of the adaptation processes. Figure 4-2 illustrates the floating-gate voltage change due to charge-coupling errors. V_X and V_Z represent charge-coupling errors for tunneling and injection, respectively. Numerical results of the simulation are shown in Table 4-1. The charge-coupling error can be reduced by increasing the total floating-gate capacitance, although this also slows down the adaptation process.

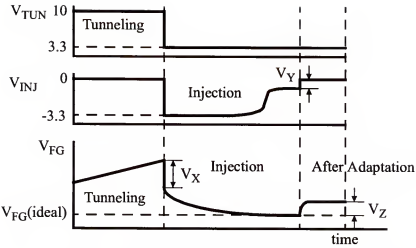


Figure 4-2. Charge-coupling errors in the adaptation process of a floating-gate adaptation circuit.

Table 4-1. Simulation results of charge-coupling errors in a floating-gate current adaptation circuit.

I_{BIAS}	C_{FG}	$V_{FG,Ideal}$	Tunnel.	Injection	$\Delta V_{FG,TUN}$	V_X	V_Z
100 nA	2 pF	2.87 V	10 msec	10 msec	0.059 mV	-116.3 mV	1.620 mV
100 nA	2 pF	2.87 V	100 msec	1 sec	0.583 mV	-116.3 mV	0.236 mV
100 nA	10 pF	2.87 V	1 sec	1 sec	1.276 mV	-24.85 mV	82.2 μV
100 nA	10 pF	2.87 V	1 sec	10 sec	1.276 mV	-24.85 mV	3.1 μV

4.2.2 Floating-Gate Quantized Adaptation Algorithm

To remove the performance degradation of adaptation circuits caused by charge-coupling errors, a new algorithm called floating-gate quantized adaptation (FGQA) is proposed. As shown in Figure 4-3, the basic idea of the FGQA technique is that the comparison and adaptation phases are separated using a clock signal. The comparison between a target value and a present value is always performed in a

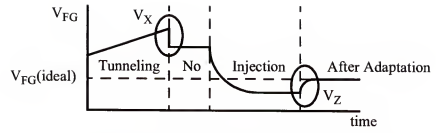


Figure 4-3. The basic concept of a floating-gate quantized adaptation circuit. The charge coupling errors do not affect the final value.

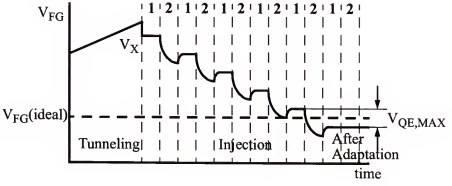


Figure 4-4. Adaptation process of a floating-gate quantized adaptation circuit. The clock period limits the quantization error.

static state after turning off tunneling and injection voltage sources. Therefore, in the comparison phase, the present voltage in the floating gate, which includes charge-coupling errors, is compared to the target voltage, and the final adapted floating-gate voltage is free from charge-coupling errors.

Figure 4-4 shows the adaptation process of a FGQA circuit, where number "1" and "2" denote the comparison and adaptation phases. In Figure 4-4, $V_{QE,MAX}$ denotes the maximum quantization error, which depends on the injection current level and the injection time step, which is half of the period of the applied clock

frequency. The quantization error is unavoidable, but it can be reduced to a much smaller value by decreasing the injection current level. However, decreasing injection current using a lower injection voltage ($V_{INJ,ON}$) increases adaptation time. Quantization error will be analyzed in Section 4.3.1.

4.2.3 Floating-Gate Quantized Adaptation Current Source

Figure 4-5 shows a current source in which the output current (I_{D2}) is adapted to an ideal value (I_B) using the FGQA technique. By forcing V_1 to V_B through a switched-capacitor feedback loop, the floating-gate voltage (V_{FG}) is adapted to an optimized value so that the output current (I_{D2}) can be compensated to equal the bias current (I_B).

Operation of the FGQA current source is similar to that of the FGA circuit shown in Figure 4-1. However, for the FGQA current source, comparison and injection processes are separated by the clock signal through additional injection control blocks. The switched-capacitor feedback loop in the FGQA current source includes a latched comparator and an injection control block, and performs comparison while V_{CLK1} is high and injection while V_{CLK1} is low. After adaptation, the Injection-Select signal (V_{IS}) and the Adaptation-Select signal (V_{AS}) go to low, by which the whole adaptation circuit becomes inactive. Schematics of the control blocks are shown in Figure 4-6 and Figure 4-7. Figure 4-8 shows control signal flows in the FGQA current source.

Simulation results for the FGQA current source using IBM6HP 0.25μm parameters are summarized in Table 4-2. In the simulation, V_{TUN} = 7 V, V_{INJ} = -3.0 V, V_{DD} = 3.3 V, and V_{SS} = 0 V were used with a 10 kHz clock. The final output

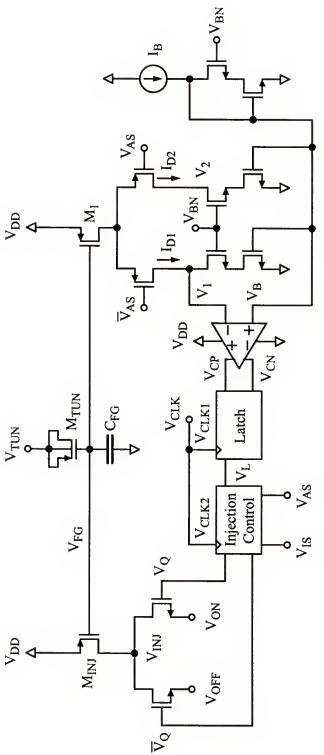


Figure 4-5. A floating-gate quantized adaptation current source.

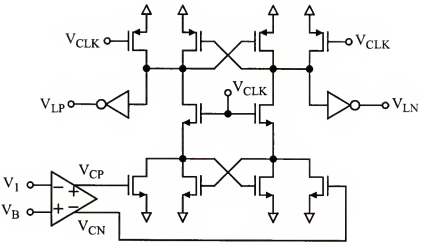


Figure 4-6. The latched comparator in the FGQA current source.

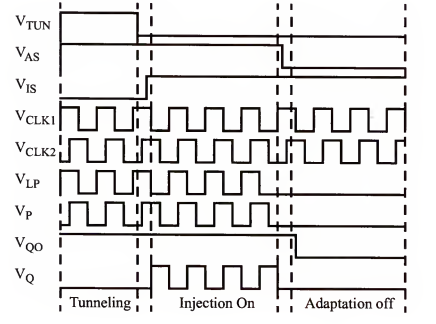
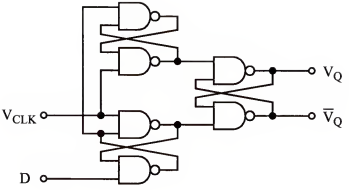


Figure 4-8. The control signal flows in the FGQA current source.



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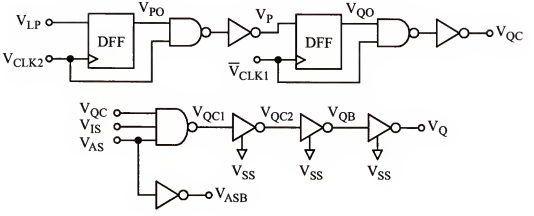


(B)

Figure 4-7. The injection control block in the FGQA current source. (A) Edge-triggered D flip-flop (ETDFF). (B) Injection control signal generator.

Table 4-2. Simulation results of the FGQA current source.

	Ideal Value	Adapted Value	% Error
V_{FG}	2.7676 V	2.7757 V	0.29 %
I_D	1 μV	1.0013 μV	0.13 %

current after quantized adaptation shows a 0.13 % error. This error could be further reduced if a higher V_{INJ} or a higher frequency clock were used to reduce the injection current level and the injection time step. However, in the simulation, a smaller V_{INJ} was used to reduce the time needed for the transient simulation.

As discussed so far, the FGQA current source can provide an extremely precise matched current, because it significantly reduces charge-coupling errors occurring when the adaptation circuit is turned off. Another useful feature of the FGQA technique is that the accuracy is controllable to fit any desired specifications, because the accuracy of the FGQA circuit is determined externally by the injection voltage and the clock frequency.

4.3 Analysis of Floating-Gate Quantized Adaptation Circuits

4.3.1 Quantization Error Analysis

In this section we will analyze quantization errors in FGQA circuits and compare the results to conventional mismatch reduction techniques.

A FGQA circuit includes unavoidable quantization error terms. The quantization error directly depends on the injection current determined by the injection voltage and the injection time step. This provides useful advantages of the FGQA technique. If slow adaptation is allowed, the FGQA technique does not have a theoretical limitation in accuracy, because of a trade-off between the quantization

error and the adaptation time period. Therefore, if the injection voltage and the clock signal are applied from an external voltage source, the quantization error (also, the accuracy of the circuit) can be controlled externally after fabrication.

The quantization error of a FGQA circuit is

$$V_{QE} \doteq \frac{I_{INJ}\Delta t}{C_{FG,\,Total}}, \tag{4.1}$$

where V_{QE} is the quantization error, I_{INJ} is the injection current, Δt is the injection time step given by $1/(2F_{CLK})$, and $C_{FG,Total}$ is the total capacitance of a floating-gate node.

A series of simulations using the FGQA current source shown in Figure 4-5 were performed. The injection time step is 50 μsec (10 kHz clock), and the total floating-gate capacitance including parasitics is 0.55 pF. As shown in Table 4-3, the simulated quantization errors of the floating-gate voltage ($V_{QE,S}$) match the estimated value using Equation (4.1) ($V_{QE,E}$). In data sets 1 and 2, the output currents show relatively large errors, because the quantization errors were intentionally enlarged by using low $V_{INJ,ON}$ for convenient simulations. In Set 4, with relatively high $V_{INJ,ON}$ the quantization error of the output current is 0.1 %.

The quantization error can also be controlled by changing clock frequencies. Set 2 and Set 5 show the simulation results with clock frequencies of 10 kHz and 100 kHz. Because the clock frequency changes to 10 times faster, the quantization error of the floating-gate voltage is reduced to about one tenth, as estimated by Equation (4.1).

4.3.2 Comparison of Mismatch Reduction

The performance of the FGQA circuit can be evaluated by comparing total chip areas along with the accuracy of the simulation in Section 4.3.1 to those of conventional mismatch reduction techniques which use large devices and array structures of unity-size devices discussed in Section 2.2.

In the FGQA technique, the total transistors used to implement a FGQA current source is about 150. Considering that minimum-size transistors were used, the total chip area can be estimated as about 900 μm^2 including adaptation control blocks, and about 1000 μm^2 for ten FGQA current sources.

To extract the results from conventional approaches, the Pelgrom model reviewed in Section 2.2.2 is applied to a typical mismatch measurement data. If we

Table 4-3. Simulation results of the quantization errors of a FGQA current source.

Set	1	2	3	4	5
Clock Frequency	10 kHz	10 kHz	10 kHz	10 kHz	100 kHz
$V_{INJ,ON}$	- 3.3 V	- 3.3 V	- 2.8 V	- 2.5 V	- 3.3 V
$V_{INJ,OFF}$	0 V	1 V	2 V	1 V	1 V
I_{INJ}	68.0 pA	74.4 pA	25.2 pA	10.9 pA	74.0 pA
$V_{FG,Final}$	2.87 V	2.87 V	2.87 V	2.87 V	2.87 V
V_{QE} by Eq.(4.1)	6.2 mV	6.8 mV	2.3 mV	1.0 mV	0.7 mV
% Error of $V_{QE,E}$	0.22 %	0.24 %	0.08 %	0.03 %	0.02 %
V_{QE} by simulation	6.1 mV	6.8 mV	1.4 mV	0.2 mV	0.6 mV
% Error of $V_{QE,S}$	0.21%	0.24 %	0.05 %	0.01 %	0.02 %
$I_{OUT,S}$	110 nA	115 nA	100.8 nA	100.1 nA	100.4 nA
% Error of $I_{OUT,S}$	10 %	15 %	0.8 %	0.1 %	0.4 %

Table 4-4. Total areas of one matched current mirror pair to achieve typical mismatch errors $(\mu m)^2$.

Error	1.0 %	0.5 %	0.2 %	0.1 %	0.01 %
Large Device	200	800	5000	20×10^3	2×10^6
Array (V_{GS}=0.5)	220	880	5500	22×10^3	2.2×10^6
Array (V_{GS}=1)	17	68	425	1700	170×10^3
FGQA	900	900	900	900	900

Table 4-5. Total areas of ten matched current mirror pairs to achieve typical mismatch errors $(\mu m)^2$.

Error	1.0 %	0.5 %	0.2 %	0.1 %	0.01 %
Large Device	1000	4000	25×10^3	100×10^3	10×10^6
Array (V_{GS}=0.5)	1100	4400	27.5×10^3	110×10^3	11×10^6
Array (V_{GS}=1)	85	340	2125	8500	850×10^3
FGQA	1000	1000	1000	1000	1000

assume that a typical 0.25 μm process has a fixed process variation of 0.25 ± 0.05 μm for width mismatch, the error of a current mirror pair that can be obtained with 900 μm^2 area is about 0.47 %. However, the error is increased to 1.49 % when ten current mirrors are used in the circuit. Also, when array structures are used, the error for a current mirror pair with 900 μm^2 is estimated as 0.49 % for V_{GS} = 0.5 V, and 0.15 % for V_{GS} = 1 V. Table 4-4 and Table 4-5 show the estimated areas for several mismatch errors and mismatch reduction techniques.

As seen in the above results, although array structures are useful for implementing low-precision circuits, FGQA circuits have a great advantage in obtaining high-precision circuits with small area.

4.4 Floating-Gate Quantized Adaptation Current Source Array

4.4.1 FGQA Current Source Array Design

The FGQA current source array shown in Figure 4-9 was designed as an example of the FGQA technique. The FGQA adapts N equivalent current outputs to a fixed external bias current so that the output current can be directly applied to an n-bit thermometer-code current steering D/A converter. The adaptation control block generates N-bit control signals for the sequential adaptation of N equivalent current outputs. External injection on/off voltages and clock signals are used to adjust the adaptation resolution and the time period.

4.4.2 Simulation and Experimental Results

A FGQA current source array with N=7 is simulated using IBM6HP 0.25 μm parameters. In the simulation, a fixed bias current of 1 μA was used with 3.3 V supply voltage, and clock frequency of 10 kHz. The tunneling voltage was 7 V and the injection on/off voltages were -0.4 V and 2V. In simulation, the individual adapted current outputs have approximately 0.1 % maximum deviations compared to the fixed bias current, and has 0.005 % maximum error when the output currents are compared to the average output current. The simulation results are summarized in Figure 4-10 and Table 4-6.

To verify the above simulation results, a FGQA current source array was fabricated using the IBM6HP 0.25 μm process. The W/L ratios of PMOS and NMOS transistors used in the FGQA current source array were (5 μm / 0.5 μm) and (1 μm / 0.5 μm), respectively, and PMOS transistors of (1 μm / 0.5 μm) were used for tunneling devices. A die photo is shown in Figure 4-11. The active chip area of the array was

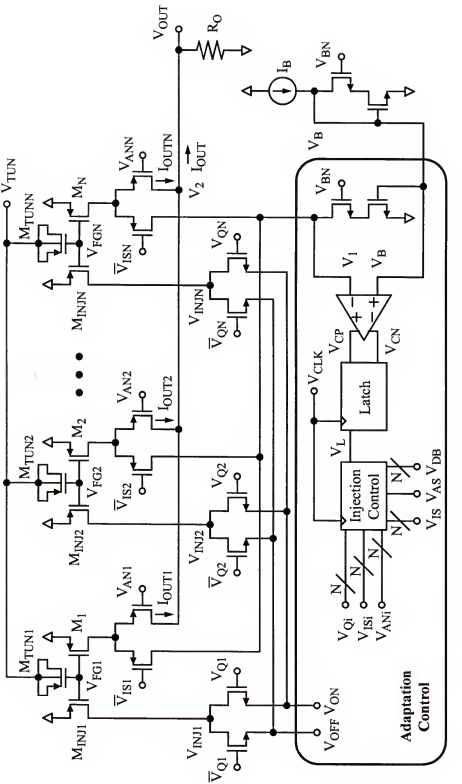
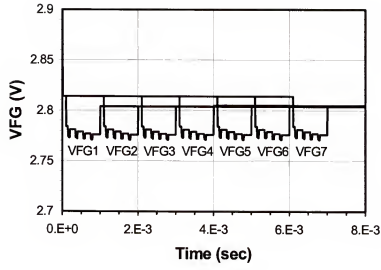
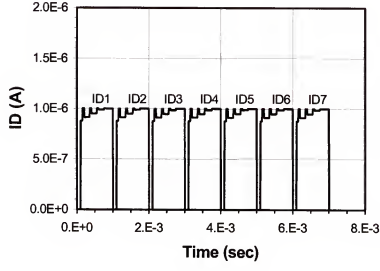


Figure 4-9. A floating-gate quantized adaptation current source array.



(A)



(B)

Figure 4-10. Simulation results of 7 equivalent output currents in the FGQA current source array. Each V_{FG} and I_D are adapted sequently. (A) Adapted floating-gate voltages (V_{FG}). (B) Adapted drain currents (I_D).

Table 4-6. Simulation results of the 7 equivalent current source array designed by using the FGQA technique with an 1 μA fixed bias current. The errors are mainly caused by quantization errors

Current Sources	Simulation Result	Error
I_{OUT1} (μA)	1.00089 μA	0.0046 %
I_{OUT2} (μA)	1.00094 μA	0.0004 %
I_{OUT3} (μA)	1.00094 μA	0.0004 %
I_{OUT4} (μA)	1.00094 μA	0.0004 %
I_{OUT5} (μA)	1.00094 μA	0.0004 %
I_{OUT6} (μA)	1.00095 μA	0.0014 %
I_{OUT7} (μA)	1.00095 μA	0.0014 %
I_{AVE} (μA)	1.000936 μA	

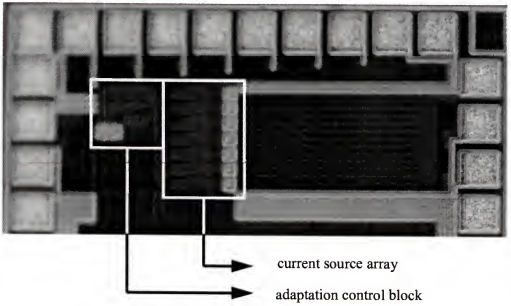


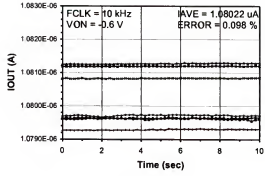
Figure 4-11. A die photo of the FGQA current source array including 7 equivalent current sources. The right side of the photo is routing lines and dummy materials.

Table 4-7. Experiment results of the adapted output currents of the FGQA 7 equivalent current source array.

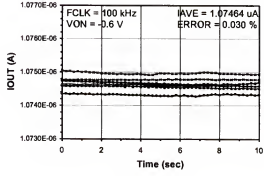
F_{CLK}	10 kHz	100 kHz	10 kHz
$V_{INJ,ON}$	- 0.6 V	- 0.6 V	- 0.4 V
I_{OUT1} (μA)	1.07962 μA	1.07467 μA	1.07444 μA
I_{OUT2} (μA)	1.07971 μA	1.07459 μA	1.07441 μA
I_{OUT3} (μA)	1.08128 μA	1.07456 μA	1.07442 μA
I_{OUT4} (μA)	1.08038 μA	1.07477 μA	1.07438 μA
I_{OUT5} (μA)	1.08119 μA	1.07497 μA	1.07445 μA
I_{OUT6} (μA)	1.07962 μA	1.07432 μA	1.07469 μA
I_{OUT7} (μA)	1.07929 μA	1.07461 μA	1.07441 μA
I_{AVE} (μA)	1.08022 μA	1.07464 μA	1.07444 μA
I_{OUT} with Max. Error	1.08128 μA	1.07497 μA	1.07469 μA
Max. Error from I_{AVE}	0.098 %	0.030 %	0.013 %

0.064 mm^2. The adapted currents were measured using a fixed bias current of 1 μA, 10 kHz and 100 kHz clock frequencies, external tunneling voltage of about 7 V, the injection-on voltages of -0.4 ~ -0.6 V, and the injection-off voltage of 3.3 V. The measured adapted current outputs of the FGQA current source array are summarized in Table 4-7.

Table 4-7 and Figure 4-12 shows the experiment results of the adapted output currents using F_{CLK} = 10 kHz and $V_{INJ,ON}$ = -0.6 V, F_{CLK} = 100 kHz and $V_{INJ,ON}$ = -0.6 V, and F_{CLK} = 10 kHz and $V_{INJ,ON}$ = -0.4 V. Mean of the measured current is 8 % above the nominal 1.00 μA. This offset was occurred by the input offset voltage of the comparator in the adaptation control loop, and it gives minor effects to the equivalent current source array. The maximum deviation from the mean is less than



(A)



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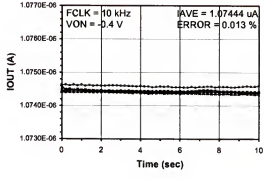


(C)

Figure 4-12. the measured output currents of the FGQA 7 equivalent current source array. (A) 10 kHz clock frequency and -0.6 V injection voltage. (B) 100 kHz clock frequency and -0.6 V injection voltage. (C) 10 kHz clock frequency and -0.4 V injection voltage.

0.1 %. The measured current outputs had smaller errors when using higher clock frequencies and higher injection voltages, because the higher clock frequency and the higher injection voltage can reduce quantization errors, as shown in Equation (4.1).

In the adaptation procedure, careful control of tunneling is strongly desired. If the tunneling procedure is done for too long, then the floating-gate voltage will be increased too much, and the injection process will require a very long time, because the injection current depends on the drain current of injection MOS devices. Estimation of the required tunneling time using tunneling model parameters [Ser04] can prevent this problem.

Recently, a floating-gate adaptation technique which can be applied to large array structures was reported [Ser04]. In the technique, the injection current of each floating-gate element in the array is determined from the period and voltage of an injection pulse, which are obtained by control circuits placed on an external PC board. The technique allows relatively short adaptation time, and is useful for adaptating large array structures, because the injection conditions are varying. However, the adaptation technique in [Ser04] requires large external circuits and is less precise than the FGQA shown here. In addition, the accuracy of injection parameters, which are used to calculate the injection condition, can be a dominant factor to determine the precision of the technique.

4.5 Conclusion

Floating-gate adaptation using charge storage on floating-gate MOS transistors can remove analog mismatch errors caused by fabrication processes

including process parameter variations. Precise control of the charge on the floating gate can be achieved by Fowler-Nordheim tunneling and impact-ionized hot-electron injection. However, charge-coupling errors caused by turning off the tunneling and injection circuitry degrades the final accuracy of the adapted quantity.

A new floating-gate quantized adaptation (FGQA) technique is proposed to compensate mismatch errors in analog circuits. The FGQA technique improves the accuracy of floating-gate adaptation circuits by removing these charge-coupling errors. The accuracy of FGQA circuits can be traded for programming time, because the quantization error is controlled by the injection current and the injection period.

As a practical example of the FGQA technique, a current source array of 7 equivalent adapted current outputs is designed, simulated, and measured using IBM6HP 0.25 μm process. Experiments show that the equivalent output currents of the FGQA 7 equivalent current source array have less than 0.1 % errors in nominal conditions, even though only minimum geometry MOS transistors were used, which produce 5 % current mismatch without adaptation. The accuracy of the FGQA circuit can also be improved further by extending the adaptation time.

CHAPTER 5
LOW-VOLTAGE QUASI-FLOATING GATE TECHNIQUE

5.1 Introduction

Due to the charge-storage capability of floating MOS gates, floating-gate techniques have been widely used in digital memory applications, such as EPROM and EEPROM. Recently, floating-gate techniques have been applied to the continuous control of CMOS threshold voltages, with applications in low-voltage digital design [Ber97, Yan00]. Furthermore, a number of analog applications based on floating-gate techniques have been developed for analog amplifiers [Ber01b, Ram95], tunable filters [Mun01], D/A converters [Lop99, Yin97], biomedical and neural network circuits [Dio02], and analog trimming and adaptation circuits [Fig00, Fig01b, Hyd02].

The main advantage of floating gates is to allow using capacitors as the key passive elements rather than using resistors in many applications such as voltage dividers, voltage adders, and feedback loops. In other applications, the effective threshold voltage of MOS transistors can be controlled by precharging the floating gate to a high or low potential. These analog floating-gate approaches provide useful new options for low-voltage, low-power, and high-precision analog circuit design.

A recurring problem in the floating-gate technique is how to control or program the initial charge of floating-gate nodes. Recently, to solve the floating-

gate initial-charge problem, techniques using so-called quasi- or pseudo-floating gates (QFGs) have been presented by several authors [Del94, Har02, Nae03, Ram03a, Seo04].

This QFG technique retains many of the benefits of true floating gates without need for ultraviolet exposure or high-voltage programming circuitry. The QFG transistor allows implementing ac-coupled amplifiers with gains set accurately by capacitors. The very high quasi-infinite resistors (QIRs) allow low-frequency cutoffs well below 1 Hz, which are useful in many applications. The QFG technique can also be used for low-voltage applications because a QFG transistor's effective threshold voltage can be controlled to a low value. Furthermore, such ac-coupled circuits are useful in analog low-voltage applications to allow shifting input common-mode voltage ranges, and hence, the voltage swing and dynamic range can be expanded. Also, if the operating voltage is biased accurately using a feedback loop, the QFG technique can be used in a number of precision analog applications. As we will demonstrate, the QFG technique retains many of the most useful features of real floating-gate techniques, although it does not provide the long-term charge-storage function of analog memory circuits.

In the QFG technique, one important factor is how to implement the required quasi-infinite resistors (QIRs). Several different QIR structures have been proposed [Del94, Har02, Nae03, Ram03a, Seo04]. However, there has been little comparison of the strengths and weaknesses of these structures for different applications. In this chapter, from fundamental analyses of the basic structures of QIRs, three sources of error: dc offset, signal distortion, and signal-dependent offset, are defined and

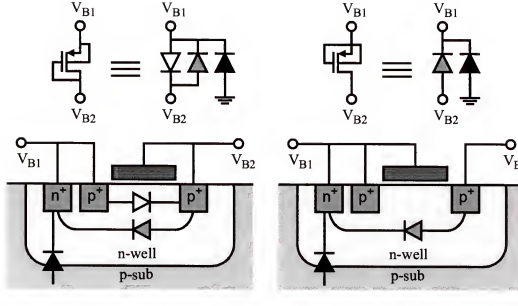


Figure 5-1. Basic structures of PMOS-based QIRs in an n-well process. (A) Gate-drain shorted QIR or GD-QIR. (B) Gate-source-bulk shorted QIR or GS-QIR.

compared for various QIR structures. Then, the suitability of different structures of QIRs in various circuits are compared using simulations and experiments. A particular QIR structure is near-optimal for many applications. Some QFG application circuits will be suggested as examples.

5.2 Quasi-Infinite Resistors

5.2.1 Basic Structures of Quasi-Infinite Resistors

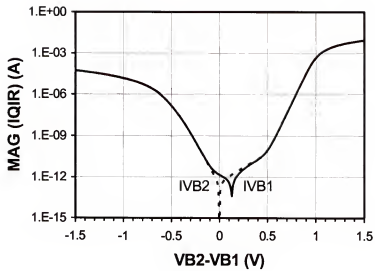
Figure 5-1 illustrates fundamental structures used in PMOS-based QIRs available in an n-well process. One such fundamental structure is the diode-connected (gate-drain shorted) PMOSFET, symbolized in Figure 5-1 using the unfilled diode symbol. Another is the parasitic lateral PNP BJT diode formed from

the p+/n-well junction in the PMOSFET, symbolized by the shaded diode. The n-well/p-substrate diode, symbolized by the filled diode, is a parasitic structure, whose leakage current can significantly affect device operation, as we shall see.

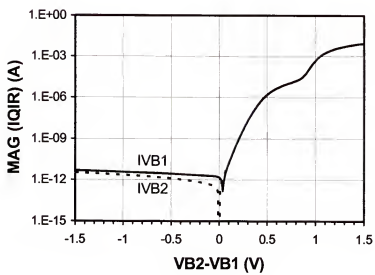
Figure 5-1(A) is a single diode-connected PMOS QIR as proposed in [Har02], in which gate and drain nodes are shorted together and source and bulk nodes are shorted together. All three of the fundamental structures are combined in this QIR. Typical bidirectional I-V curves of this gate-drain-shorted QIR (GD-QIR for short) are shown in Figure 5-2(A). The magnitudes of the QIR currents are plotted on a log scale. In a typical QFG application, one of the voltages V_{B1} or V_{B2} is fixed, and the other becomes a QFG node. Ideally, in the steady state, the QFG voltage is pulled to the fixed voltage. When an ac input is applied, the QFG voltage follows the ac input. When V_{B1} is larger than V_{B2}, the PMOS diode is forward-biased and the BJT diode is reverse-biased, and vice-versa. Note in Figure 5-2(B) that the current of the GD-QIR is not symmetric for forward- and reverse-bias conditions.

Figure 5-1(B) shows the gate-, source-, and bulk-shorted PMOS QIR (GS-QIR) proposed in [Nae03]. In this case, the PMOS diode current is mostly eliminated since the gate and source are shorted, and only the parasitic lateral PNP BJT diode from drain to bulk and the parasitic n-well/p-substrate diode are significant. Therefore, the I-V curves in Figure 5-2(B) are even more asymmetric than the curves in Figure 5-2(A).

QIRs can also be implemented using NMOSFETs [Ram03b]. In a p-well process, an NMOS-based QIR has the same characteristics as a PMOS-based QIR.



(A)



(B)

Figure 5-2. Simulations of I-V curves of PMOS-based QIRs in an n-well process. (V_{B1}=1.5V and V_{B2}=0~3V, dc sweep). (A) GD-QIR. (B) GS-QIR.

However, NMOS-based QIRs in a single n-well process cannot be used because bulk nodes of all NMOSFETs are shorted together unless a twin-well process is used. When the ground voltage (the most negative voltage) is applied as a fixed bias of all QIRs in a circuit, a single NMOS-based QIR can be used with an n-well process because all of the source and bulk nodes in the QIRs have the same potential.

5.2.2 Error Terms in Quasi-Infinite Resistors

Typically, our goal in using a QIR in an ac-coupled circuit is to force the QFG dc voltage to a desired bias, while allowing the QFG voltage to follow ac inputs. However, because of substrate-diode currents and asymmetric QIR currents, the QFG voltage deviates from this desired behavior. From the analysis of QFG input circuits, the errors can be classified into dc offset, signal distortion, and signal-dependent offset.

If the QFG node is connected to the substrate-diode end of a QIR, the well-substrate reverse-bias leakage current must flow through forward bias diodes in the QIR, causing a dc offset. The magnitude of this offset is difficult to predict, but can be substantial. To reduce the offset, the n-well/p-substrate junction area should be minimized, but such scaling cannot eliminate all offset. (The offset does disappear, however, if the voltage across the well-substrate junction is zero, as occurs in some applications.)

Now, suppose an ac input is applied. The instantaneous QFG voltage follows the ac input, and diodes within the QIR can conduct on signal peaks, causing distortion. The circuit effectively integrates any net current flowing onto the QFG

node. Any asymmetry in the positive and negative currents will produce a time-dependent QFG voltage shift with a signal-dependent integration time. We call this voltage shift signal-dependent offset.

5.3 Comparison of Quasi-Infinite Resistor Structures

Figure 5-3 introduces a simplified symbol for QIRs and shows some possible QIR structures. The QIR symbol shown in Figure 5-3(A) can represent either GD- or GS-QIRs. The arrow in the QIR symbol is used to indicate the location of the well-substrate diode and the direction of the substrate leakage current. Figure 5-3(B)~(E) show ac-coupled input circuits with four different types of QIR connections: single, parallel, series, and voltage-divider connections, each of which could use GD- or GS-QIRs.

The input circuit with the single QIR, as shown in Figure 5-3(B), is the simplest connection, and was used with the GD-QIR structure in [Ram03a]. The single-QIR connection with the substrate diode connected to the bias voltage V_B avoids all dc offset. The diode currents of a GD-QIR are more balanced than those of the GS-QIR. Thus, the signal-dependent offset with a GD-QIR is smaller. However, the allowed QFG undistorted voltage swing with the GD-QIR is also smaller, typically limiting swings to less than about 0.7 V_{PP}.

Figure 5-3(C) shows an input circuit with parallel-connected QIRs. The enhanced symmetry of this connection improves signal distortion and signal-dependent offset, but is still subject to dc offset because of substrate current, and the voltage swing is even more limited.

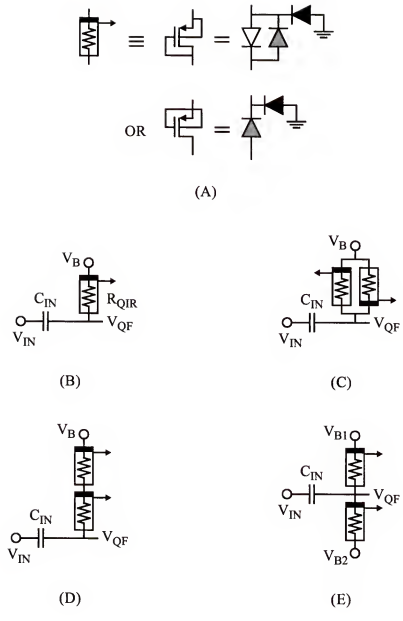


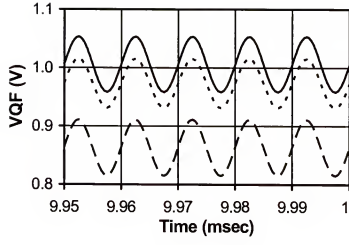
Figure 5-3. A QIR symbol and ac-coupled input circuits with possible QIR structures. (A) The QIR symbol of GD- and GS-QIRs, where the arrow indicates the location of the well-substrate diode and the direction of the substrate leakage current. (B) Single. (C) Parallel. (D) Series. (E) Voltage-Divider.

Table 5-1. THD, offset, and signal reduction of QFG voltages in ac-coupled input circuits with single-, parallel-, and series-connected QIRs.

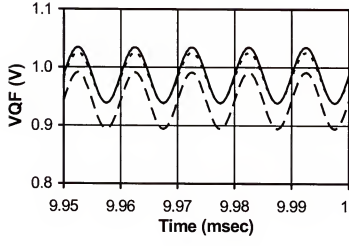
QIRs	GD-QIR (V_B=1V)			GS-QIR (V_B=1V)		
	THD (dB)	offset(mV)	sig. red. (%)	THD (dB)	offset(mV)	sig. red. (%)
single	-40.2	5.5	5.3	-38.8	-13.6	4.2
parallel	-33.7	-26.8	16.2	-36.4	-18.2	13.6
series	-21.8	-137	4.3	-29.3	-57.4	3.0
QIRs	GD-QIR (V_B=0V)			GS-QIR (V_B=0V)		
	THD (dB)	offset(mV)	sig. red. (%)	THD (dB)	offset(mV)	sig. red. (%)
single	-45.3	5.8	5.1	-40.1	-13.4	3.4
parallel	-45.2	-2.4	17.7	-45.5	-1.9	15.1
series	-45.6	5.1	4.4	-44.9	-1.7	3.4

As reported in [Har02], series-connected QIRs, as shown in Figure 5-3(D), can be used to increase QFG voltage swings. Since the series-connected QIRs have smaller but more asymmetric diode currents, they have lower signal distortion but larger signal-dependent offset. With this connection, dc offset due to substrate leakage is unavoidable.

HSPICE transient simulations of several ac-coupled input circuits, using several QIR connections, are shown in Table 5-1. The simulations used model parameters from the IBM 6HP process. In each simulation, an input signal of 0.5 V dc and 100 mV_{PP} ac is applied through a 100 fF input capacitor. Minimum-size PMOSFETs (0.8 μm/0.24 μm) were used in the QIRs, and the area and the perimeter of the n-well were 7.84 x 10^{-12} m^2 and 11.84 μm. The simulation results in Figure 5-4 and Table 5-1 are consistent with the previous analysis. Single GD-QIRs gave

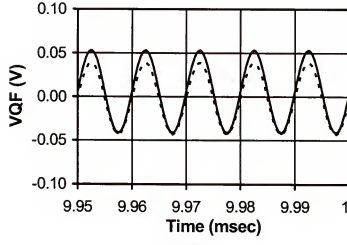


(A)

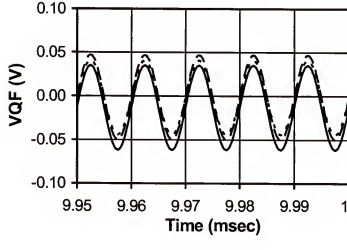


(B)

Figure 5-4. QFG voltages connected to a fixed bias in an ac-coupled input circuit (solid line; single, dotted line; parallel, and dashed line; series connections). (A) GD-QIR, V_B=1V. (B) GS-QIR, V_B=1V. (C) GD-QIR, V_B=0V. (D) GS-QIR, V_B=0V.



(C)



(D)

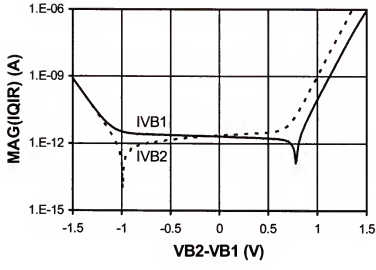
Figure 5-4. Continued.

smaller signal distortion than GS-QIRs. The parallel connections have the smallest signal-dependent offset but produce large dc offsets and significantly reduced voltage swing. The series connections had the small signal distortion and large voltage swing, but both dc and signal-dependent offsets were relatively large.

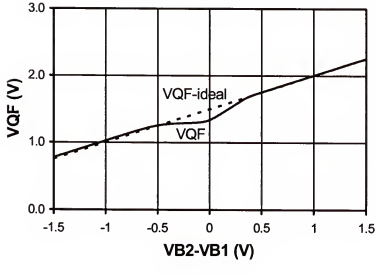
Therefore, the best selection of a QIR depends on the circuit application. For precision, low-signal-swing circuits, single GD-QIRs tend to provide the best results, as they are free of dc offset, and exhibit fairly symmetric currents. When larger ac signals are required but dc offset is not important, parallel and series connections may be better choices.

Another interesting QIR structure is the voltage-divider connection shown in Figure 5-3(E). In Figure 5-3(E), the QFG node is connected to two different fixed bias voltages through QIRs, as proposed in [Nae03]. In [Nae03], when different bias sources are applied to the upper and lower biases, the QFG dc voltage is determined by voltage division between two QIRs, and significant undistorted QFG voltage swings are possible. However, since the diode currents of the QIRs are unequal, it is difficult to predict the ultimate QFG voltage.

A series of measurements were made on voltage-divider connections using both GD- and GS-QIRs in the AMI 0.5 μm process. In the experiments, one terminal (V_{B1}) in Figure 5-3(E) was fixed at 1.5 VDC, while the other terminal (V_{B2}) was swept from 0 to 3 V. The substrate was fixed at 0 V. The QFG voltage was monitored using a voltage follower, and the V_{B1} and V_{B2} currents were measured. Figure 5-5 shows the results. With both QIRs the QFG voltage differs from (V_{B1} + V_{B2})/2 by up to 150 mV. Thus, this connection is poorly suited for applications in

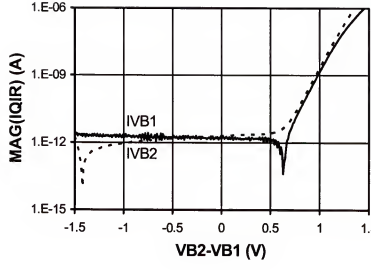


(A)

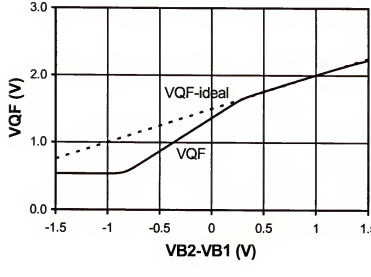


(B)

Figure 5-5. The experiment results of the QIR currents and QFG voltages of voltage-divider QIRs shown in Figure 5-3(E). (A) I_{QIR} of a GD-QIR. (B) V_{QF} of a GD-QIR. (C) I_{QIR} of a GS-QIR. (D) V_{QF} of a GS-QIR.



(C)



(D)

Figure 5-5. Continued.

Table 5-2. Summary of comparison results of QIR structures.

	dc offset	signal distortion	signal-dep. offset	voltage swing	current balance
single	O	Δ	O	X	O
parallel	X	Δ	O	X	O
series	XX	O	X	O	X
voltage-divider	XX	X	X	O	X

* O: good, Δ: medium, X: worse, and XX: worst.

which the QFG voltage needs to be accurately set. The comparison results of four different QIR structures shown in Figure 5-3 are summarized in Table 5-2.

5.4 Applications of Quasi-Floating Gate Technique

5.4.1 Closed-Loop Quasi-Floating Gate Circuit

Because of the unpredictable offsets of QIRs, the operating points in the foregoing circuits can be hard to control. Many of these problems are avoided if the QIRs are used to provide dc feedback [Nae03]. Figure 5-6 shows a closed-loop ac coupled QFG amplifier in which the QIR pulls the dc operating point of a QFG node

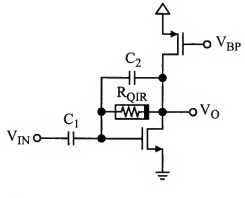


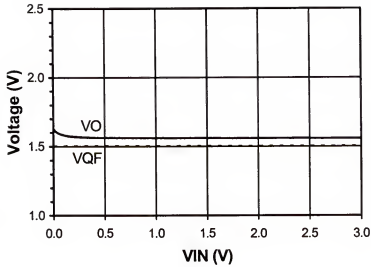
Figure 5-6. A quasi-floating gate closed-loop capacitive-coupled NMOS amplifier which has a dc feedback loop provided by a quasi-floating resistor.

close to the output dc voltage, and both ac and dc feedback loops provide stable operation. The capacitor ratio of C_1 to C_2 sets the amplifier ac gain. Note that in such circuits, the effects of substrate-diode leakage current can be minimized by connecting the substrate diode to the output node.

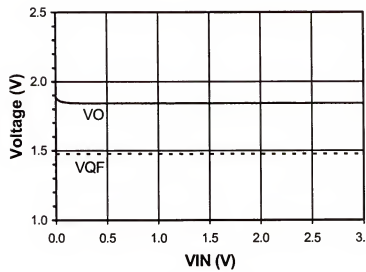
The output-voltage swing of such amplifiers can be significantly limited. As in the circuit of Figure 1 in [Nae03], series-connected QIRs can be used to increase output swing. However, as in previous examples using such series connections, offsets due to substrate leakage become unavoidable. Simulations and experiments show that input-output voltage differences can exceed several hundred mV. Fortunately, the offset appears at the output and usually is not critical. However, in very low-voltage circuits, the reduction in output headroom could be significant.

To observe the dc and transient offsets of closed-loop QFG amplifiers, two QFG amplifiers with parallel-connected (Figure 5-3(C)) and series-connected (Figure 5-3(D)) GD-QIRs were fabricated using minimum geometry in the AMI 0.5 μm process.

Figure 5-7 shows experimental results of dc offset voltages between QFG and output nodes of closed-loop QFG amplifiers as in Figure 5-6 with parallel-connected (Figure 5-3(C)) and series-connected (Figure 5-3(D)) GD-QIRs. As shown in Figure 5-7, the amplifier with series-connected QIRs was much higher output-referred dc offset than the amplifier with parallel-connected QIRs. Figure 5-8 shows ac transient measurements of the same amplifiers. For the amplifier with parallel-connected GD-QIRs, Figure 5-8(A) shows significant distortion for ac input voltage larger than 0.8 V_{PP}. Measured THDs were -34, -28, and -20 dB for input

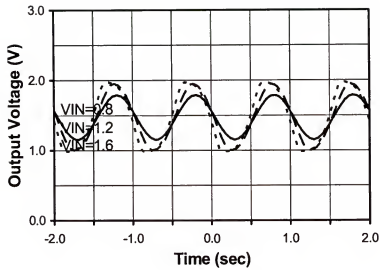


(A)

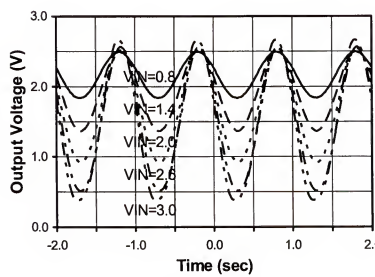


(B)

Figure 5-7. The experiment results of dc offset voltages between QFG and output nodes of closed-loop QFG amplifiers shown in Figure 5-6. (A) Parallel-connected GD-QIRs. (B) Series-connected GD-QIRs.



(A)



(B)

Figure 5-8. The experimental results of ac transient measurements of ac-coupled closed-loop QFG amplifiers. (A) Parallel-connected GD-QIRs. (B) Series-connected GD-QIRs.

signals of 0.8, 1.2, and 1.6 V_{PP}. Signal-dependent offset was about 3 mV when the input was 1.6 V_{PP}. In Figure 5-8(B), the amplifier with series-connected GD-QIRs had much larger signal-dependent offset, although large voltage swing with low distortion was possible. When the input was 3.0 V_{PP}, THD was measured as -23 dB. However, the signal-dependent offsets were 228, 456, and 710 mV when the inputs were 1.4, 2.0, and 3.0 V_{PP}, respectively.

5.4.2 Low-Voltage Quasi-Floating Gate Circuit

In low-voltage analog circuit design, because of the reduced supply voltage, the common-mode voltage range and voltage swing of analog input circuits and analog switch circuits are significantly limited. To relieve these limitations, it is usually necessary to reduce the threshold voltage or to use complicated voltage boosting techniques. However, threshold voltage reduction and voltage boosting techniques may increase gate leakage currents, and overall performance can be significantly degraded.

The QFG technique is useful in such low-voltage applications. By connecting the QFG node to a fixed-bias supply voltage, the effective threshold voltage of a FET for ac signals can be shifted up and down. Such connections make it easy to match input and output bias levels, and hence, allow voltage swings and dynamic ranges to be can be expanded.

Many floating-gate application circuits can easily be modified to equivalent QFG versions. The detailed discussion of the QFG application circuits will be in Chapter 6.

5.5 Conclusion

A variety of possible structures can be used to implement the quasi-infinite resistances (QIRs) used in the quasi-floating gate (QFG) technique. The choice of a QIR structure for a given application typically involves performance trade-offs balancing dc offset, signal-dependent offset and undistorted signal swing.

The QFG technique provides many useful features in low-voltage applications. For low-voltage applications with a supply voltage less then two diode turn-on voltages, a single PMOS QIR provides best performance for biasing a quasi-floating node without any dc offset. By using the QIRs, the QFG node can be precisely biased to well-defined dc operating point without any common-mode voltage problems which limit the supply voltage reduction in low-voltage analog circuits.

The QFG technique also retains many of the advantages of real floating-gate techniques for adaptive circuit elements and capacitive-computational circuits, although it does not have long-term charge-storage ability for analog memory elements. Many QFG application circuits can be implemented from well-known useful floating-gate circuits by applying minor modifications. Some example QFG circuits were proposed.

CHAPTER 6
APPLICATIONS OF QUASI-FLOATING GATE CIRCUITS

6.1 Introduction

Floating-gate techniques have been widely used in many applications for several decades, not only for both digital [Ber97, Yan00] and analog circuits, especially for low-voltage, low-power, and high-precision analog applications [Ber01b, Dio02, Fig01b, Hyd02, Ram95, Yin97]. As mentioned in Chapter 5, the quasi-floating gate (QFG) technique [Del94, Har02, Nae03, Ram03a, Seo04] can be used to control the initial charge of the floating-gate node without using complicated additional circuits or external high voltages.

In this chapter, the design method of QFG circuits and some design examples of the QFG versions of useful floating-gate circuits will be proposed. In Section 6.2, floating-gate multiple-input translinear element (FG MITE) applications such as geometric-mean, squaring-reciprocal, and multiply-divide circuits will be reviewed, and QFG versions of the FG MITE circuits will be proposed by adding QIRs. Section 6.3 will introduce QFG MITE 1st- and 2nd-order CMOS log-domain filters. In Section 6.4, a fully-differential operational amplifier with QFG common-mode feedback and a D/A converter will be discussed. In Section 6.5, we will present experimental results of selected QFG application circuits, including a QFG MITE geometric-mean circuit and a fully-differential operational amplifier with QFG common-mode feedback (CMFB).

6.2 QFG Multiple-Input Translinear Element

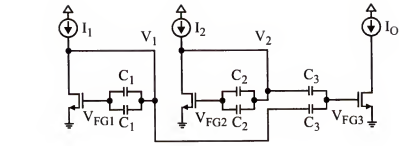
The translinear principle relates a product-of-power law constraint in the current domain to a linear constraint on the voltages in a circuit based on the exponential current-voltage characteristics of bipolar transistors [Gil75]. Circuits based on the translinear principle include analog multipliers [Gil83, Hui82], current conveyors, [Fab85, Nor85], frequency multipliers [Ash76, Kon79, Sur88], and current amplifiers [Fab88, Tou89]. Subthreshold-operated MOS transistors also provide the translinear exponential current-voltage characteristics, and so can be used in translinear applications [Enz99, Pyt96, Tou94]. Using floating-gate MOS transistors in subthreshold mode widely expands the applications of translinear circuits [Min96].

Several floating-gate multiple input translinear element (FG MITE) circuits have been proposed [Min98, Ram01]. In this section, we will examine some MITE signal processing circuits, and describe a simple method to convert them to the QFG versions.

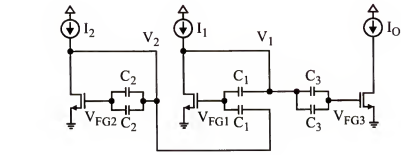
Figure 6-1 shows some examples of FG MITE signal processing circuit blocks. The output currents of each circuits in Figure 6-1(A), (B), and (C) are geometric-mean, squaring-reciprocal, and multiply-divide of the input currents [Min98, Min01], as shown in Equation (6.1), Equation (6.2), and Equation (6.3).

$$I_{O,GM} = \sqrt{I_1 I_2}. \tag{6.1}$$

$$I_{O,SR} = I_1^2 I_2. \tag{6.2}$$



(A)



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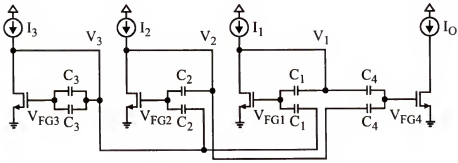


(C)

Figure 6-1. Examples of floating-gate multiple-input translinear element (FG MITE) circuits. (A) A FG MITE geometric mean circuit ($I_O=(I_1I_2)^{1/2}$). (B) A FG MITE squaring-reciprocal circuit ($I_O=I_1^2/I_2$). (C) A FG MITE multiply-divide circuit ($I_O=I_1I_2/I_3$).

$$I_{O,MR} = I_1 I_2 / I_3 . \tag{6.3}$$

The initial charge of floating gates of the FG MITE circuits must set to balanced values by using any initialization procedure. The MITE circuits reported in [Min01] used the UV-conductance method to set the initial floating-gate charge. The UV-conductance method is inconvenient compared to QFG techniques, which provide a circuit-based initialization method by forcing well-defined operating points on floating gates through quasi-infinite resistors (QIRs).

Figure 6-2 shows proposed quasi-floating gate versions of multiple-input translinear element (QFG MITE) circuits, where the resistor symbol enclosed a box denotes a QIR, and the side including a thick line in the box represents the direction of a well-substrate junction in a QIR. The QFG MITE circuits in Figure 6-2 have the same functions as the FG MITE circuits shown in Figure 6-1.

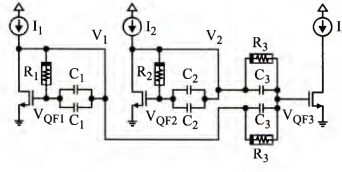
To find a correct connection of a QIR, we need to consider dc signals in static state. There are various ways to connect QIRs that ensure stable dc operation of QFG circuit. However, if the QIRs are connected to mimic at dc the operation of the circuit at ac, then circuits' bias points will work for both ac and dc.

In the static state with fixed dc current inputs, the drain currents of input transistors in the geometric-mean circuit in Figure 6-2(A) are given by

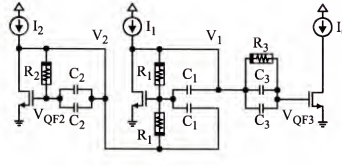
$$I_1 = I_0 e^{(KV_{QF1})/V_T}, \tag{6.4}$$

$$I_2 = I_0 e^{(KV_{QF2})/V_T}, \tag{6.5}$$

where K is the number of inputs in a multiple-input transistor, V_{QFi} is a floating-



(A)



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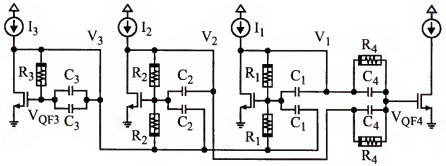


(C)

Figure 6-2. Quasi-floating gate multiple-input translinear element (QFG MITE) circuits. (A) A QFG MITE geometric mean circuit ($I_O=(I_1I_2)^{1/2}$). (B) A QFG MITE squaring-reciprocal circuit ($I_O=I_1^2/I_2$). (C) A QFG MITE multiply-divide circuit ($I_O=I_1I_2/I_3$).

gate voltage, and V_T is the thermal voltage. The output current can be presented by

$$I_O = I_0 e^{(KV_{QF3})/V_T}, \tag{6.6}$$

$$I_O = I_1 e^{[K(V_{QF3} - V_{QF1})]/V_T} = I_2 e^{[K(V_{QF3} - V_{QF2})]/V_T}, \tag{6.7}$$

$$I_O^2 = I_1 I_2 e^{[K(2V_{QF3} - V_{QF1} - V_{QF2})]/V_T}. \tag{6.8}$$

Therefore, when the QFG node voltages are balanced as

$$2V_{QF3} = V_{QF1} + V_{QF2}, \tag{6.9}$$

the output current will be the geometric-mean of two input currents as seen in Equation (6.1).

Now, let's consider the constraint of QFG node voltages. If we neglect any parasitic capacitance, the QFG voltages are obtained by the charge on quasi-floating capacitors in static state and capacitance coupling relations, such as

$$V_{QF1} = \frac{2C_1V_1 + Q_1}{2C_1} = V_1 + \frac{Q_1}{2C_1}, \tag{6.10}$$

$$V_{QF2} = \frac{2C_2V_2 + Q_2}{2C_2} = V_2 + \frac{Q_2}{2C_2}, \tag{6.11}$$

$$V_{QF3} = \frac{C_3V_1 + C_3V_2 + Q_3}{2C_3} = \frac{V_1 + V_2}{2} + \frac{Q_3}{2C_3}. \tag{6.12}$$

Where Q_1, Q_2, and Q_3 are the stored-charge in the capacitors, C_1, C_2, and C_3, respectively. Substituting Equation (6.10), Equation (6.11), and Equation (6.12) to Equation (6.9), the constraint in Equation (6.9) becomes

$$\frac{Q_3}{C_3} = \frac{Q_1}{2C_1} + \frac{Q_2}{2C_2}, \tag{6.13}$$

where Q_1 and Q_2 are

$$Q_1 = 2C_1(V_{QF1} - V_1), \tag{6.14}$$

$$Q_2 = 2C_2(V_{QF2} - V_2). \tag{6.15}$$

In static state, Q_1 and Q_2 will be zero if we connect V_{QF1} to V_1 and V_{QF2} to V_2 using QIRs. From Equation (6.13), Q_3 also becomes zero, and Equation (6.10), Equation (6.11), and Equation (6.12) can be

$$V_{QF1} = V_1, \tag{6.16}$$

$$V_{QF2} = V_2, \tag{6.17}$$

$$V_{QF3} = \frac{V_1 + V_2}{2}. \tag{6.18}$$

Therefore, in the geometric-mean circuit, four QIRs should be connected between V_{QF1} and V_1, V_{QF2} and V_2, V_{QF3} and V_1, and V_{QF3} and V_2.

The other QFG MITE circuits in Figure 6-2(B) and (C) also have similar constraints with the geometric-mean circuit, and we can find the constraints in the same way. The QFG MITE squaring-reciprocal circuit shown in Figure 6-2(B) requires to satisfy

$$2V_{QF1} = V_{QF2} + V_{QF3}, \tag{6.19}$$

$$V_{QF1} = \frac{V_1 + V_2}{2}, \tag{6.20}$$

$$V_{QF2} = V_2, \tag{6.21}$$

$$V_{QF3} = V_1, \tag{6.22}$$

while the constraints of the multiply-divide circuit shown in Figure 6-2(C) is

$$V_{QF1} + V_{QF2} = V_{QF3} + V_{QF4}, \tag{6.23}$$

$$V_{QF1} = \frac{V_1 + V_3}{2}, \tag{6.24}$$

$$V_{QF2} = \frac{V_2 + V_3}{2}, \tag{6.25}$$

$$V_{QF3} = V_3, \tag{6.26}$$

$$V_{QF4} = \frac{V_1 + V_2}{2}. \tag{6.27}$$

Therefore, four and seven QIRs should be used in the squaring-reciprocal and multiply-divide circuits, respectively.

The QFG MITE circuits shown in Figure 6-2 were designed as described above, and simulated using IBM6HP 0.25 μm model parameters. The W/L ratios of PMOS and NMOS transistors used in the circuit were (400 μm / 1.2 μm) and (100 μm / 1.2 μm), respectively. And, PMOS transistors of (1.5 μm / 0.6 μm) with a minimum n-well were used for implementing QIRs.

In the practical design of QFG MITE circuits, the QIRs should be selected carefully with considerations of signal swing at QFG nodes because of the wide signal range of translinear elements. For an example, if we need to use 4 decades of current range (100 pA ~ 1 μA), the voltage swing at a QFG node is estimated about

500 mV in a typical 0.25 μm process. Since the voltage swing allowed in a single QIR is about 100 ~ 200 mV as seen in Chapter 5, the QIRs should be used in series-connection of four QIRs.

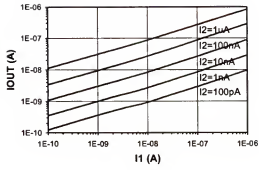
Figure 6-3 presents simulated output currents of QFG MITE geometric-mean, squaring-reciprocal, and multiply-divide circuits in Figure 6-2 when input currents are changed from 100 pA to 1 μA. The output currents of the QFG MITE circuits were well matched to the desired arithmetic functions of the input currents.

6.3 QFG MITE CMOS Log-Domain Filter

Log-domain filtering is a promising approach for implementing electronically tunable integrated continuous-time current-mode filters [Fox00]. Log-domain filters use the translinear principle to cancel nonlinearity [Gil90, Fre93], and the use of exponential current versus voltage characteristics offers a high transconductance to current ratio [Enz99]. The log-domain approach can also be efficiently combined with class-AB operation to extend the dynamic range [Fox00, Pyt01].

Log-domain filters can be implemented using MOS transistors biased in weak inversion, avoiding the base current of bipolar transistors [Enz99, Pyt96, Tou94]. On the other hand, maintaining the MOS transistors in weak inversion usually requires large devices and limits response. Another limitation of CMOS log-domain circuits is threshold voltage mismatch which can considerably degrade linearity [Pyt01].

Log-domain filters can also be implemented using FG MITE networks [Min99]. In the time domain, a 1st-order low-pass filter is described by



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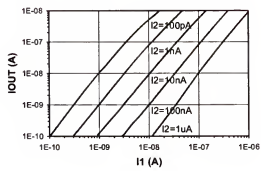

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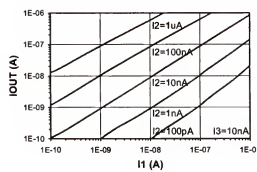


(C)

Figure 6-3. Simulation results of QFG MITE circuits. (A) A QFG MITE geometric mean circuit ($I_O=(I_1I_2)^{1/2}$). (B) A QFG MITE squaring-reciprocal circuit ($I_O=I_1^2/I_2$). (C) A QFG MITE multiply-divide circuit ($I_O=I_1I_2/I_3$).

$$y + \tau\frac{dy}{dt} = x, \tag{6.28}$$

where x and y are the input and output of the filter, and τ is the time constant of the filter. If we assume that the input and output signals of the filter are represented as ratios of signal currents to a unit current, Equation (6.28) can be rewritten as

$$I_y + \tau\frac{dI_y}{dt} = I_x, \tag{6.29}$$

where $x = I_x/I_i$ and $y = I_y/I_i$. The drain current of a CMOS transistor in subthreshold operation is given by

$$I_y = I_0 e^{-KV_y/V_T}, \tag{6.30}$$

and to find time derivative of the current, we can write

$$\frac{dI_y}{dt} = \frac{dI_y}{dV_y}\frac{dV_y}{dt} = \left(-\frac{K}{V_T}I_y\right)\frac{dV_y}{dt}. \tag{6.31}$$

Substituting Equation (6.31) into Equation (6.28), we can get

$$I_y + \tau\left(-\frac{K}{V_T}I_y\right)\frac{dV_y}{dt} = I_x, \tag{6.32}$$

$$\frac{I_x}{I_y} = 1 - \left(\frac{K\tau}{CV_T}\right)\left(C\frac{dV_y}{dt}\right). \tag{6.33}$$

Now, we introduce a capacitor current, I_c, a time-constant current, I_τ, and an auxiliary current, I_p, such as

$$I_\tau \equiv \frac{CV_T}{K\tau}, \tag{6.34}$$

$$I_c \equiv C\frac{dV_y}{dt}, \tag{6.35}$$

$$I_p \equiv I_\tau - I_c. \tag{6.36}$$

Substituting Equation (6.34) ~ Equation (6.36) to Equation (6.33),

$$\frac{I_x}{I_y} = 1 - \frac{I_c}{I_\tau} = \frac{I_p}{I_\tau}, \tag{6.37}$$

$$I_p = \frac{I_x I_\tau}{I_y}. \tag{6.38}$$

Therefore, we can obtain the translinear loop equations from Equation (6.38),

$$I_p I_y = I_x I_\tau, \tag{6.39}$$

$$I_\tau = I_p + I_c. \tag{6.40}$$

From the translinear loop equations given by Equation (6.39) and Equation (6.40), a 1st-order low-pass FG MITE log-domain filter can be implemented as shown in Figure 6-4 [Min02]. A simple analysis of the translinear loop of the circuit in Figure 6-4 can be obtained by using floating-gate voltages and drain currents. If

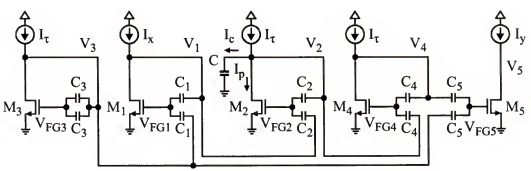


Figure 6-4. A 1st-order low-pass floating-gate multiple-input translinear element (FG MITE) CMOS log-domain filter.

all of the floating-gate capacitors in the circuit are equal, from Equation (6.30), we can get

$$\ln I_y = -\frac{KV_y}{V_T}\ln I_0 = -\frac{KV_{FG5}}{V_T}\ln I_0 \equiv 2AV_{FG5}, \tag{6.41}$$

$$A \equiv -\frac{K}{2V_T}\ln I_0. \tag{6.42}$$

Floating-gate voltage V_{FG5} is obtained by the same way as in the QFG MITE circuits in Section 6.2.

$$V_{FG5} = \frac{V_4 + V_3}{2} \tag{6.43}$$

Therefore, from Equation (6.41) and Equation (6.43),

$$\ln I_y = 2AV_{FG5} = A(V_4 + V_3). \tag{6.44}$$

For the other current components, we can get

$$\ln I_\tau = 2AV_{FG4} = A(V_4 + V_2), \tag{6.45}$$

$$\ln I_p = 2AV_{FG2} = A(V_2 + V_1), \tag{6.46}$$

$$\ln I_x = 2AV_{FG1} = A(V_1 + V_3). \tag{6.47}$$

Adding Equation (6.44) to Equation (6.46) and Equation (6.45) to Equation (6.47), we can obtain the translinear loop equation which is equal to the Equation (6.39).

$$\ln I_y + \ln I_p = \ln I_y I_p = A(V_4 + V_3 + V_2 + V_1), \tag{6.48}$$

$$\ln I_\tau + \ln I_x = \ln I_\tau I_x = A(V_4 + V_2 + V_1 + V_3), \tag{6.49}$$

$$\ln I_y I_p = \ln I_\tau I_x . \tag{6.50}$$

The cut-off frequency of the filter is derived from the time constant such as

$$\tau = \frac{1}{\omega_0} = \frac{C}{G_m} = \frac{KC}{g_m}, \tag{6.51}$$

$$f_0 = \frac{g_m}{2\pi KC}, \tag{6.52}$$

$$g_m = \frac{\partial I_\tau}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}}(I_0 e^{-KV_{GS}/V_T}) = \frac{K}{V_T} I_\tau, \tag{6.53}$$

The gain of the filter is determined from the ratio of input to output currents such as

$$\text{Gain} = \frac{I_y}{I_x} = \frac{G_{m5}}{G_{m1}} . \tag{6.54}$$

A 1st-order low-pass QFG MITE log-domain filter shown in Figure 6-5 can be implemented by minor modification of a FG MITE log-domain filter shown in Figure 6-4. The QFG MITE log-domain filter has the same structure as the FG MITE circuit except it includes QIRs to hold proper dc operating points on the floating gates. To ensure the same ac and dc operations, the QIRs should be

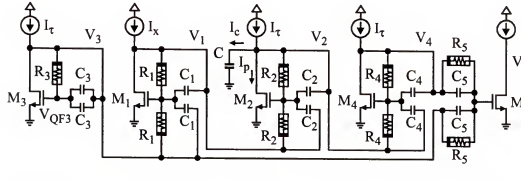


Figure 6-5. A 1st-order low-pass quasi-floating gate multiple-input translinear element (QFG MITE) CMOS log-domain filter.

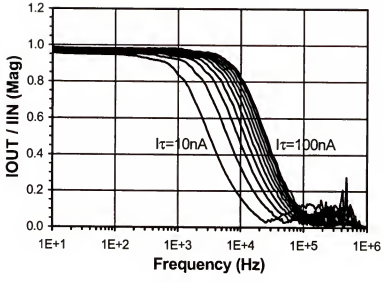
connected with careful considerations of the static state operating points discussed in Section 6.2.

In the filter design, IBM6HP 0.25 μm parameters were used with 2 V supply. The W/L ratios of PMOS and NMOS transistors were (200 μm / 1.2 μm) and (100 μm / 1.2 μm), respectively, and PMOS transistors of (1.5 μm / 0.6 μm) with a minimum n-well were used for implementing QIRs. The number of FG multiple-inputs (K) was 2, g_m was about 280 nA/V, C was 10 pF, and floating-gate capacitors of 0.2 pF were used. Also, all QIRs were used in the form of a four series-connected QIR. Figure 6-6 shows the simulation results of the 1st-order low-pass QFG MITE log-domain filter. The time constant current (I_τ) was swept 10 ~ 100 nA with a 10 nA step, and the frequency tuning range from 1.8 kHz to 15 kHz was obtained. Also, the width of output transistors was changed up to 5 times of the input transistors to obtain the gain.

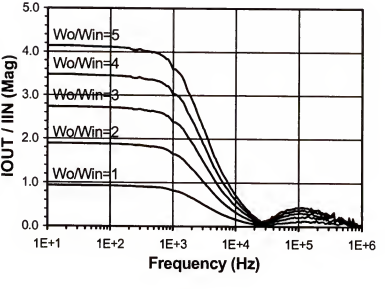
A 2nd-order QFG MITE log-domain filter can also be implemented using the same method. Figure 6-7 shows a 2nd-order low-pass FG MITE log-domain filter [Min02], and the QFG version of the filter is shown in Figure 6-8. In the 2nd-order filter, g_m was about 2.6 μA/V, C was 3 pF, and floating-gate capacitors of 0.2 pF were used. Figure 6-9 shows the simulation results of frequency and gain tuning of the 2nd-order low-pass QFG MITE log-domain filter. The time constant current (I_τ) was swept 100 ~ 1000 nA, and the frequency tuning range was from 50 to 350 kHz.

6.4 Low-Voltage QFG Fully Differential Amplifier

Figure 6-10(A) shows a QFG fully differential amplifier. The QIRs provide dc feedback between QFG nodes and output nodes to maintain stable dc common-



(A)



(B)

Figure 6-6. Simulation results of a 1st-order low-pass QFG MITE CMOS log-domain filter. (A) Frequency tuning. (B) Gain tuning.

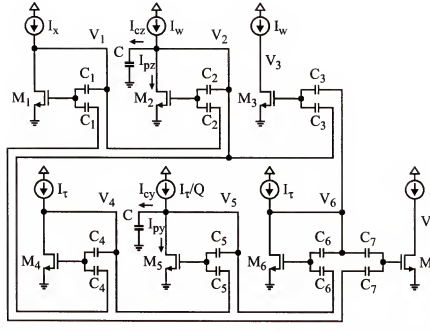


Figure 6-7. A 2nd-Order low-pass floating-gate multiple-input translinear element (FG MITE) CMOS log-domain filter.

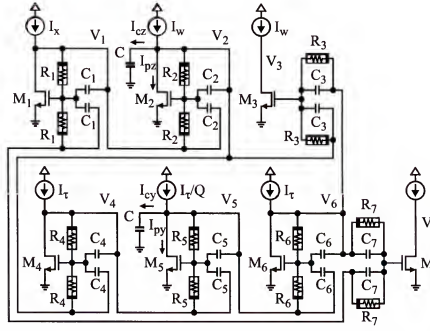
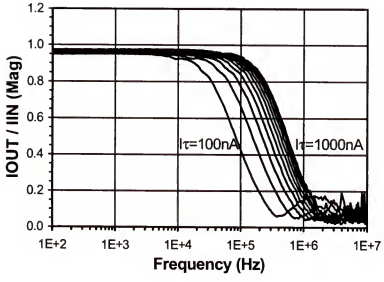
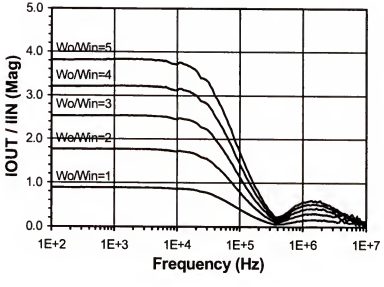


Figure 6-8. A 2nd-Order low-pass quasi-floating gate multiple-input translinear element (QFG MITE) CMOS log-domain filter.

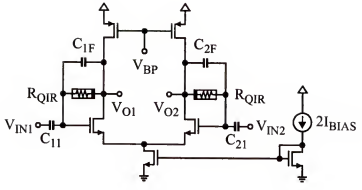


(A)

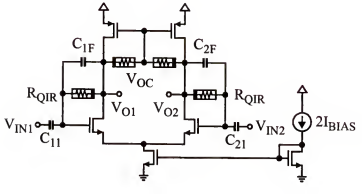


(B)

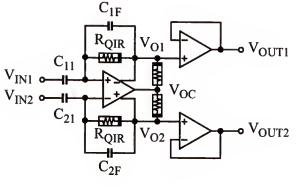
Figure 6-9. Simulation results of a 2nd-order low-pass QFG MITE CMOS log-domain filter. (A) Frequency tuning. (B) Gain tuning.



(A)



(B)



(C)

Figure 6-10. A quasi-floating gate (QFG) fully differential amplifier. (A) A QFG amplifier. (B) A QFG amplifier with QFG common-mode feedback. (C) A QFG amplifier with output buffers.

mode voltages on QFG nodes. Series-connected QIRs are available to increase voltage swing, because output dc offsets induced by well-substrate leakage currents of QIRs give minor effects in the circuit.

The QIRs can also be used to fix output common-mode voltages. Figure 6-10(B) shows a QFG fully differential amplifier with QFG common-mode feedback (CMFB). As shown in Figure 6-10(B), connecting QIRs between output nodes and an internal node which can adjust dc bias currents (the node connected to the output of a conventional CMFB circuit), the output dc common-mode voltages are forced to be stable. The QFG CMFB can reduce design complexity and chip areas of a fully differential amplifier. In the practical design, the output buffers are added at the outputs as shown in Figure 6-10(C).

Two different sets of QFG fully differential amplifiers with QFG CMFB circuits based on the structure shown in Figure 6-10(C) were simulated using AMI 0.5 μm parameters and 2 V supply voltage. The W/L ratios of PMOS and NMOS transistors were (100 μm / 1.2 μm) and (25 μm / 1.2 μm), respectively.

Three amplifiers in the first set used single, two series-connected, and four series-connected QIRs, respectively, to explore voltage swing limitations in QIRs. All QIRs in the amplifiers of the first set were implemented using minimum-size PMOS transistors of (1.5 μm / 0.6 μm). Input and feedback capacitors were fixed to 0.2 pF, and the amplifier gain was set to 0.9 by the ratio of input and feedback capacitors including parasitic capacitances.

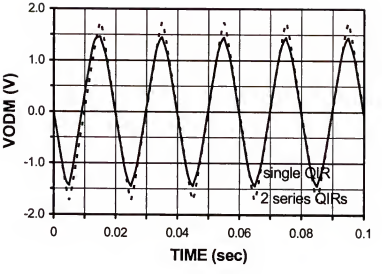
Another four amplifiers in the second set were designed with intentional mismatches to see the effects of QIR mismatch. The amplifiers in the second set

implemented using QIRs which had 10 % and 20 % larger widths on one side of a differential pair than the QIR widths in the other side for single and two series-connected QIRs.

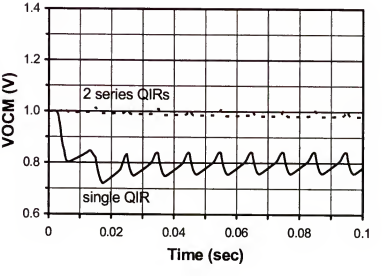
Figure 6-11(A) shows the differential output voltages of QFG fully differential amplifiers when full swing saw-tooth differential input signals are applied. The amplifier with single QIRs shows significant distortion when the differential output signal becomes larger than 2 $V_{p\text{-}p}$ because of the limited voltage swing of single QIRs. However the amplifier with two series-connected QIRs does not have voltage swing limitations, and provides almost rail-to-rail voltage swing. The amplifier which uses four series-connected QIRs (not shown in Figure 6-11(A)) shows the exactly same results as the amplifier with two series-connected QIRs. Therefore, as we have seen, when the voltage swing allowed in QIRs is not large enough, large signal distortion can occur.

The common-mode voltage can also be shifted when the voltage swing of QIRs in the QFG CMFB circuit is limited. Figure 6-11(B) shows the common-mode output voltages of QFG fully differential amplifiers with single and two series-connected QIRs. In the amplifier with single QIRs, positive peaks of the output waveform were distorted because of the small allowable voltage swing for single QIRs, and the common-mode output voltages were shifted down considerably.

Another advantage of a QFG CMFB circuit is insensitivity to the QIR mismatch between in two differential paths. The QIRs in a QFG CMFB circuit are used as dc paths to provide operating points in static state, and the operating points of both ends of a QIR are stabilized by feedback loops. Therefore, the mismatch of



(A)



(B)

Figure 6-11. The output voltages of QFG fully differential amplifiers with QFG common-mode feedback implemented using single QIRs and two series-connected QIRs. (A) Differential output voltages. (B) Common-mode output voltages.

QIRs does not affect the operating points. In simulations, the three amplifiers which have 0, 10, and 20 % mismatched QIRs in the differential pairs show the same output and differential output voltages as each others as shown in Figure 6-12. In Figure 6-12, the output voltages of the three amplifiers are superposed to the same values.

In analog circuit design, there will be numerous applications for operational amplifiers. QFG amplifiers and QFG CMFB circuits can be applied to many applications. As an example, a low-voltage 6-bit D/A converter using the QFG amplifier had been designed and simulated using AMI 0.5μm parameters and 1.5 V supply voltage as shown in Figure 6-13(A). In the D/A converter, the required total capacitance is $(2^{N+2}-2)C$. In the 6-bit design, the unit capacitor was 0.1 pF, and total accumulated capacitance was about 25.4 pF. The simulated output voltage of the

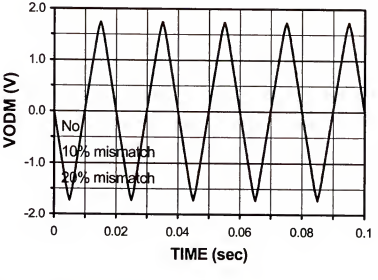
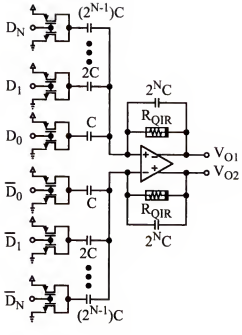
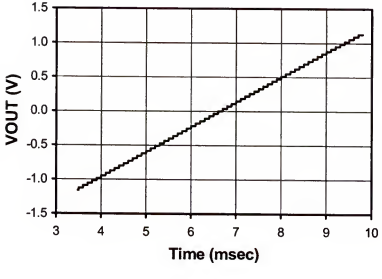


Figure 6-12. The differential output voltages of QFG fully differential amplifiers with QFG common-mode feedback including intentional mismatches.



(A)



(B)

Figure 6-13. A low-voltage D/A converter using a QFG fully differential amplifier. (A) Schematic. (B) Simulated output voltage.

QFG D/A converter is shown in Figure 6-13(B). In simulations, the integral nonlinearity (INL) and differential nonlinearity (DNL) of the D/A converter had obtained as 0.0396 LSB and 0.0328 LSB. Absolute and relative accuracies were calculated to 7.47 Bits and 6.34 Bits.

6.5 Measurement of Quasi-Floating Gate Circuits

6.5.1 QFG MITE Geometric-Mean Circuit

To verify the design method of a QFG MITE circuits, a QFG MITE geometric-mean circuit shown in Figure 6-2(A) was implemented using the AMI 0.5 μm process. The W/L ratios of PMOS and NMOS transistors in the circuit were (400 μm / 1.2 μm) and (100 μm / 1.2 μm), respectively. And, PMOS transistors of (1.5 μm / 0.6 μm) with a minimum n-well were used for QIRs. The active chip area of the circuit was 0.054 mm^2 and the supply voltage was 2 V.

The output currents of the QFG MITE geometric-mean circuit were measured as I_1 was swept between 10 nA to 430 nA with respect to the fixed I_2's of 10 nA and 100nA. As shown in Figure 6-14, the measured output currents are well matched to the geometric-mean function of the input currents. In Figure 6-14, the measured geometric-mean currents are compared to the ideal value calculated by Equation (6.1).

6.5.2 QFG Fully Differential Amplifier

A series of QFG fully differential amplifiers with QFG CMFB based on the schematic in Figure 6-10 were fabricated using the AMI 0.5 μm process. The W/L ratios of PMOS and NMOS transistors in the circuit were (100 μm / 1.2 μm) and (25 μm / 1.2 μm), respectively. And, PMOS transistors of (1.5 μm / 0.6 μm) with a minimum n-

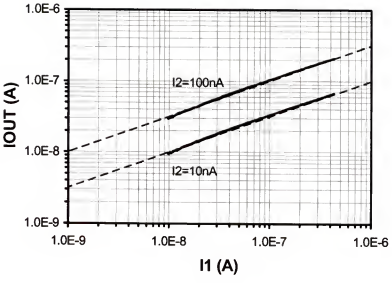
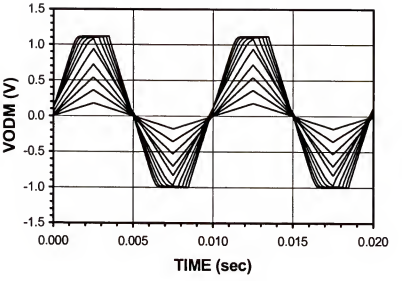


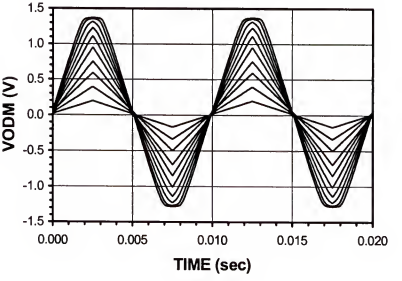
Figure 6-14. Experiment results the output currents of the QFG MITE geometric-mean circuit ($I_O=(I_1I_2)^{1/2}$). Dashed line: ideal response.

well were used for implementing QIRs. The amplifiers were implemented including different QIRs and different intentional mismatches, as mentioned in Section 6.4. The active chip area of a QFG amplifier was about 0.041 mm^2 including output buffers and 0.016 mm^2 without buffer. Input and feedback capacitors were set to a fixed value of 0.2 pF, and the supply voltage was 2 V.

Figure 6-15 shows the differential output voltages of QFG amplifiers with single and two series-connected QIRs. The 100 Hz saw-tooth wave was used for the input signal, which was swept from 1 V $\pm$ 100 mV_{PP} to 1 V $\pm$ 1 V_{PP} with a $\pm$100 mV_{PP} step. As shown in Figure 6-15, the differential output voltages show gain of 0.9 for small input signals, and begin to distort when a 1.2 V_{PP} input is applied to the single QIR amplifier, and the 1.4 V_{PP} input is applied to two series-connected QIR amplifier. The output voltage swing of the QFG amplifier with single QIRs is



(A)



(B)

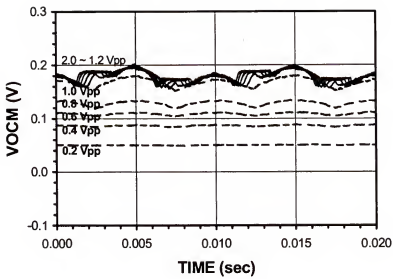
Figure 6-15. The measured differential output voltages of QFG fully differential amplifiers with QFG common-mode feedback. (A) For the amplifier with single QIRs. (B) For the amplifier with two series-connected QIRs.

2.1 V, while the voltage swing of the QFG amplifier with two series-connected QIRs is 2.65 V. The output voltage swing of the QFG amplifier with single QIRs are limited by the QIRs, and abrupt clamping of output voltages occurs for differential output signals larger than 2.1 V_{PP}, or about four times the diode turn-on voltage. For the QFG amplifier with two series-connected QIRs, the output swing is extended, but it is smaller than twice the output swing of the single-QIR case.

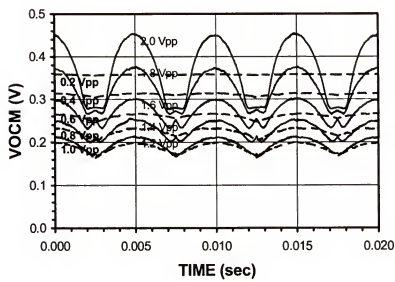
The common-mode output voltages of the QFG amplifiers are shown in Figure 6-16. When large ac input signals are applied to the QFG amplifier, either the positive or negative output voltage reaches the limit of the output swing earlier than the other side. If the positive output swing is less than the negative output swing, the common-mode voltage shifts down, and vice versa.

The output voltage swing can be increased by reducing the well-substrate junction leakage current. The output node of the QFG amplifier shown in Figure 6-10(B) is connected to two well-substrate junction; one comes from a feedback QIR and the other comes from a CMFB QIR. If the CMFB QIR is reversed, as shown Figure 6-17(A), the voltage drop caused by well-substrate leakage current can be reduced. Figure 6-17(B) shows the simulation result of output voltage swing with the QIR reversed. The output voltage swing is increased about 200 mV when the well-substrate junction of CMFB QIRs is connected to the V_{OCM} node in Figure 6-17(A).

Figure 6-18 shows the measured differential output voltages of QFG amplifiers including intentional mismatches in QIRs. The three amplifiers with 0, 10, and 20 % intentional area-mismatched QIRs show nearly identical results as

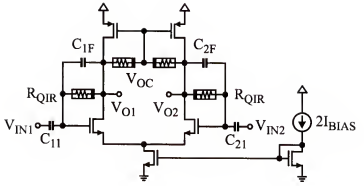


(A)

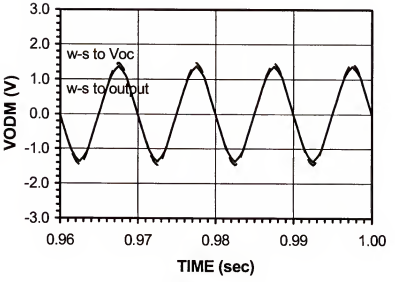


(B)

Figure 6-16. The measured common-mode output voltages of QFG fully differential amplifiers with QFG common-mode feedback. (A) For the amplifier with single QIRs. (B) For the amplifier with two series-connected QIRs.

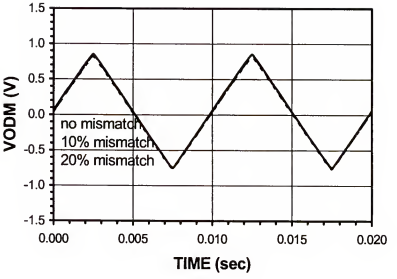


(A)

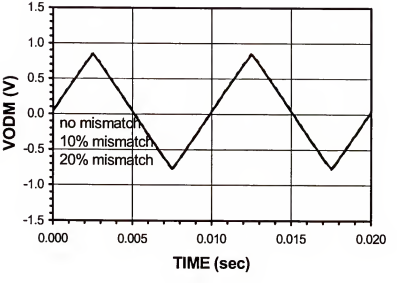


(B)

Figure 6-17. (A) A QFG fully differential amplifier with reversed QIRs in QFG CMFB. (B) Comparison of differential output voltage swing.



(A)



(B)

Figure 6-18. The measured differential output voltages of QFG fully differential amplifiers with QFG common-mode feedback including intentional mismatch in QIRs. (A) For the amplifier with single QIRs. (B) For the amplifier with two series-connected QIRs.

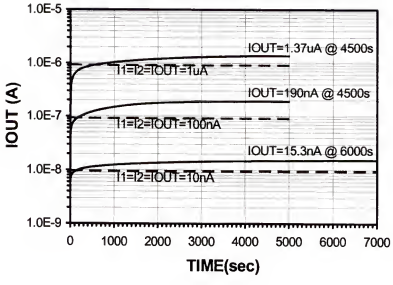
discussed in Section 6.4. Therefore, in the QFG fully differential amplifiers, the QIRs in each differential path are insensitive to mismatch. Since the QIRs are operated based on very small leakage currents, the 10 % or 20 % difference of leakage currents in mismatched QIRs cannot change operating points significantly.

6.5.3 Settling Behavior of QFG Circuits

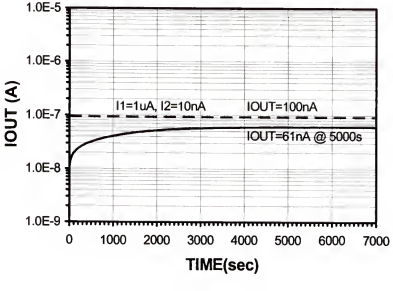
QFG circuits may have slow very settling behavior because QIRs are operated based on small leakage currents. Also, the QFG circuits will show different settling behavior for ac and dc inputs, because the operating points of QFG nodes are set by QIRs for dc input while they are set by capacitors for ac input.

Figure 6-19 shows the measurement data of the dc settling time of the QFG MITE geometric-mean circuit shown in Figure 6-2(A). In Figure 6-19(A), when the input currents were fixed to 1 μA, 100 nA, and 10 nA, the output currents were measured to 1.37 μA, 190 nA, and 15.3 nA with very long settling times, more than a hour. Also, in Figure 6-19(B), when the inputs were I_1 = 1 μA and I_2 = 10 nA, the output current was measured to 61 nA. For pure dc input, the output current shows large offset because the QIRs in the QFG MITE geometric-mean circuit use a voltage-divider QIR structure, which leads to large dc offset caused by well-substrate leakage currents, as discussed in Chapter 5.

Figure 6-20 shows the measured ac settling time of the QFG MITE geometric-mean circuit. In the geometric mean circuit shown in Figure 6-2(A), one current input (I_1) was varied from 10 nA to 430 nA with 0.1Hz input frequency and the other input current (I_2) is fixed to 10 nA. Figure 6-20(A) shows the transient characteristic and Figure 6-20(B) shows the input and output currents after settling

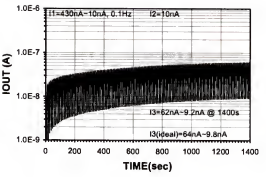


(A)

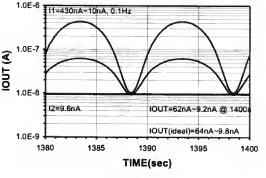


(B)

Figure 6-19. The measurement data of the dc settling time of the QFG MITE geometric-mean circuit. (A) $I_1 = I_2 = 1$ μA, 100 nA, and 10 nA. (B) $I_1 = 1$ μA and $I_2 = 10$ nA.



(A)



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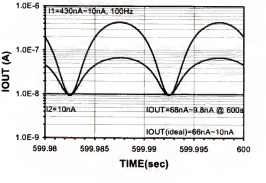

(C)

Figure 6-20. The measured ac settling time of the QFG MITE geometric-mean circuit. (A) Settling in time-domain for 0.1 Hz input. (B) Settled currents for 0.1 Hz input. (C) Settled currents for 100 Hz input.

for 0.1 Hz input current. Figure 6-20(C) shows the input and output currents after settling for 100 Hz input current. The settling time is reduced when the signal frequency is increased but it is still very long. These long settling time can be a big problem in QFG circuits, and it needs to be improved. However, QFG fully differential amplifiers show fast settling behavior when an ac input is applied. Furthermore, the QFG circuits are mostly based on capacitive computational, and hence, they are used for ac signals.

The settling time of a QIR can be analyzed by using a simple model. For a forward-biased diode used as a QIR, connecting a capacitor C to a voltage source V_A, with initial capacitor voltage V_O, the time to settle to within a tolerance V_X (> about 2 thermal voltages V_T) of V_A is given approximately by

$$I_S e^{V/V_T} = C\frac{dV}{dt} \tag{6.55}$$

$$\frac{I_S dt}{C} = e^{-V/V_T} dV \tag{6.56}$$

$$\int_{T_1}^{T_2} \frac{I_S}{C} dt = \int_{(V_A - V_O)}^{V_X} e^{-V/V_T} dV \tag{6.57}$$

$$T_X = \left(\frac{CV_T}{I_S}\right)\left[e^{-V_X/V_T} - e^{(V_O - V_A)/V_T}\right], \tag{6.58}$$

where I_S is the diode saturation current. If V_A - V_O is more than a few times the thermal voltages the first term in Equation (6.58) dominates and the log of the error decreases linearly with time. For C = 1 pF, I_S = 1e-14 A, V_T = 0.025 V, (CV_T/I_S) = 2.5 seconds, and the circuit reaches 200 mV of its final value in T_X = 2.5exp(-200/

25) = 840 μsec. It gets within 100 mV in 2.5exp(-4)= 45 msec. It reaches 50 mV of its final value in about 2.5exp(-2) = 0.33 seconds. After that it gets even slower, as the reverse leakage becomes significant. If we assume very small reverse leakage current such as I_S goes to 1e-18 A, (CV_T/I_S) becomes 25000 seconds, and for V_X = 50 mV, T_X will be about one hour. Also, note that any ac signal superposed on the dc will tend to speed things up, because such a small leakage current does not appear.

6.6 Conclusion

Because QFG techniques retain many useful features of real floating-gate techniques except the long-term charge-storage function of analog memory circuits, quasi-floating gate (QFG) techniques can apply to many useful floating-gate applications with minor modification of conventional floating-gate circuits.

Several selected examples of QFG applications have been introduced and analyzed. The design methods of QFG multiple-input translinear element (MITE) circuits are introduced, and application circuits, such as geometric-mean, squaring-reciprocal, and multiply-reciprocal circuits, have been implemented as design examples. Also, the design methods of QFG CMOS log-domain filters have been discussed and the first- and second-order low-pass QFG CMOS log-domain filters are designed.

A QFG fully differential amplifier with QFG common-mode feedback and a QFG D/A converter have been proposed. The proposed QFG amplifier has a continuous-time capacitive-coupling input circuit which can relieve the limitation of the input common-mode voltage range in low-voltage applications. The new QFG

common-mode feedback circuit can replace conventional CMFB circuits and retains useful advantages, such as the reduction of design complexity, small circuit area, and insensitivity to QIR mismatches. A low-voltage 6-bit D/A converter using a QFG amplifier is shown as an application of the QFG fully differential operational amplifier.

Experiments of selected QFG circuits showed very long dc settling behavior with large dc offset. This long settling time can be a serious practical problem in QFG circuits. The settling time is reduced when the QFG circuit uses ac inputs or closed-loop structures. Because QFG circuits are based on capacitor coupling, the dc offset occurred by QIRs can be a minor problem.

CHAPTER 7
SUMMARY AND SUGGESTIONS FOR FUTURE WORK

7.1 Summary

Due to the development of advanced deep sub-micron process technologies, the importance of low-voltage and low-power analog design techniques has significantly increased. This research focuses on design techniques for low-voltage and low-power analog circuits based on several new techniques, including standard, floating-gate, and quasi-floating gate MOS transistors with standard CMOS process technologies. These include current-mode techniques, switched-capacitor analog filters using charge-transfer amplifiers and integrators, floating-gate quantized adaptation, and quasi-floating gate techniques using quasi-infinite resistors.

In Chapter 2, the details of low-voltage and low-power limitations and trade-offs with analog mismatch were discussed, and some low-voltage and low-power circuits were proposed. A low-voltage current-mode bandgap reference which can be operated with sub-1 V supply was proposed as an alternative to conventional bandgap reference circuits, which cannot be used with very low supply voltages. The minimum supply voltage is about 0.9 V with low threshold voltage devices, and 1.2 V with normal threshold voltage CMOS transistors. The proposed current-mode bandgap reference was simulated temperature sensitivity of 74 ppm/^{o}C in the temperature range of -10 ~ 125 ^{o}C.

Also, a new class of low-power switched-capacitor filter architectures based on charge-transfer integrators was introduced. The proposed charge-transfer switched-capacitor filters can be used for very low power applications due to the low-power operation of charge-transfer amplifiers and integrators. To demonstrate the proposed filters, first-order and second-order lowpass and second-order bandpass filters were designed and simulated using minimum-geometry CMOS transistors. The proposed charge-transfer analog filter can achieve extremely low-power operation, very low static power consumption, and insensitivity to bias conditions. The power dissipation of the first-order, the second-order lowpass and second-order bandpass filters are 0.20, 0.46, and 0.66 μW, respectively, for 50 kHz clock frequency.

In Chapter 3, fundamental principles of floating-gate and multiple-input floating-gate MOS transistors were reviewed for low-voltage and low-power applications. Floating-gate circuits can be used to design continuous-time capacitive-computational circuits, which use capacitors as precise elements, unlike resistor-based circuits or switched-capacitor circuits. Three techniques, UV-conductance processing, Fowler-Nordheim tunneling plus hot-electron injection, and quasi-floating gates, were also discussed as ways to achieve precise control of floating-gate charge. A circuit for extracting tunneling and injection parameters was implemented to determine the simulation parameters of floating-gate adaptation circuits.

In Chapter 4, a new floating-gate quantized adaptation technique was proposed. The technique can greatly reduce analog mismatch errors. As an example,

a precise current source array with 7 equivalent current sources was implemented using a standard 0.25 μm CMOS process. Simulations and experiments showed that the output currents of the floating-gate quantized adaptation current source array have less than 0.1 % errors on nominal conditions, even though only minimum geometry MOS transistors were used, which produce 5 % mismatch without adaptation. The accuracy which mainly depends on the quantization error can be improved further by extending the adaptation time.

In Chapter 5, several recently reported structures for quasi-infinite-resistors were compared. Error terms, limitations, and applications of quasi-floating gate techniques were also discussed. The quasi-floating gate technique retains many of the most useful features of real floating-gate techniques, although it does not provide the long-term charge-storage. The choice of a quasi-infinite resistor structure for a given application involves performance trade-offs balancing dc offset, signal-dependent offset and undistorted signal swing.

In Chapter 6, some selected application circuits of quasi-floating gate techniques were introduced and analyzed. Methods for designing quasi-floating gate multiple-input translinear-element circuits and quasi-floating gate CMOS log-domain filters were discussed. Also, a quasi-floating-gate fully differential amplifier with a simple quasi-floating gate common-mode feedback and a quasi-floating-gate D/A converter were proposed. The proposed quasi-floating gate amplifier has a continuous-time capacitive-coupling input circuit which can relieve the limitation of input common-mode voltages in low-voltage applications. The new quasi-floating gate common-mode feedback circuit can replace conventional

common-mode feedback circuits, and retains useful advantages such as the reduction of design complexity and circuit areas. The dc and ac settling behavior were analyzed. In the experiments of selected QFG circuits, very long dc settling behavior with large dc offset was observed. This long settling time can be a serious practical problem in QFG circuits. The settling time is reduced when the QFG circuit uses ac inputs or closed-loop structures.

7.2 Suggestions for Future Work

The floating-gate quantized adaptation technique discussed in Chapter 4 still suffers relatively complicated circuitry. Recently, two interesting adaptation techniques have been announced. One is the adaptation technique for large array structures [Ser04], while another is a technique which eliminates tunneling process [Won04]. The former uses a technique similar to quantized adaptation since it includes discrete steps for its injection process. The adaptation time is reduced very much and rapid programming can be achieved because the injection voltage and period are changed for each step. However, it includes very large external circuits and computer-based calculation procedure for the calculation of injection conditions. The latter technique is quite simple compared to the former technique or the quantized adaptation because it doesn't use tunneling process, although, performance and suitability of the technique have not been verified in detail yet. Therefore, it will be worthwhile to reduce the complexity of adaptation algorithm and circuitry for any of the three techniques.

Although many useful analyses and applications were discussed in Chapters 5 and 6, the technique could be applied to many more places. In Chapter 6, only

some selected examples of quasi-floating gate multiple-input translinear elements and CMOS log-domain filters had been introduced. There should be many other translinear elements and higher order log-domain filters which can be candidates of quasi-floating gate applications. Because of the simplicity of quasi-floating gates, quasi-floating gate fully differential amplifiers and quasi-floating gate common-mode feedback circuits will also provide a wide range of application areas, especially for low-voltage applications and large array structures. Beside the circuit introduced in Chapter 6, quasi-floating gate techniques may be useful to implement many alternatives of low-voltage bias circuit blocks.

However, the settling behavior discussed in Section 6.5.3 can significantly limit the QFG applications. Therefore, a continuous attempt to find out the way to improve settling behavior and to verify useful quasi-floating gate applications which can replace and upgrade the current practical circuits is recommended.

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BIOGRAPHICAL SKETCH

Inchang Seo was born in Kimhae, Korea, in 1966. He received B.S. and M.S. degrees in physics from Hanyang University, Seoul, Korea, in 1988 and 1990, respectively. He also received an M.S. degree in electrical and computer engineering from the University of Florida, Gainesville, Florida, in 2000. He is currently pursuing a Ph.D. degree as a graduate research assistant at the University of Florida.

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His main research interests involve low-voltage, low-power, high-precision analog and mixed-signal integrated circuit design including low-voltage wide-band $\Delta\Sigma$ data converters, precise bias circuit blocks, low-power charge transfer amplifiers and filters, floating-gate CMOS analog circuits, and quasi-floating gate analog applications. Upon graduation he will join Samsung Electronics in Suwon, Korea, as a principal research engineer.

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